The Dark Side of Flyback Converters

Presented by Christophe Basso

Senior Scientist
IEEE Senior Member
Course Agenda

- The Flyback Converter
- The Parasitic Elements
- How These Parasitics Affect your Design?
- Current-Mode is the Most Popular Scheme
- Fixed or Variable Frequency?
- More Power than Needed
- The Frequency Response
- Compensating With the TL431
What is the Subject?

- There has been numerous seminars on Flyback converters
- Seminars are usually highly theoretical – link to the market?
- Industrial requirements usually not covered: standby, over power…
- This 3-hour seminar will shed lights on less covered topics:
  - Why the converter delivers more power than expected? Solutions?
  - Books talk about compensation with op amps, I have a TL431!
  - The origin of the Right-Half Plane Zero, how do I deal with it?
  - Quasi-resonant converters presence increases, how do they work?
  - In a 3-hour course, we are just scratching the surface…!
The Flyback, a Popular Structure

- The flyback converter is widely used in consumer products
- Ease of design, low-cost, well-known structure
  - Poor EMI signature, bulky transformer, practical up to 150 W

- **DVD player**
  - Flyback \( \approx 10 \text{ – } 35 \text{ W} \)

- **Set-top box**
  - Flyback \( \approx 3 \text{ – } 5 \text{ W} \)

- **Charger**
  - Flyback \( \approx 3 \text{ – } 5 \text{ W} \)

- **Notebook**
  - Flyback \( \approx 40 \text{ – } 180 \text{ W} \)

- **Netbook**
  - Flyback \( \approx 40 \text{ – } 180 \text{ W} \)
An Isolated Buck-Boost

- The flyback converter is derived from the buck-boost cell

- The addition of a transformer brings:
  - Up or down scale $V_{in}$
  - Isolation
  - Polarity change
  - More than 1 output
The Turn-on Event

- The power switch turns on: current ramps up in $L_p$, $D$ is blocked.

- The current increases in the inductor in relationship to $V_{in}$ and $L_p$.

- The output capacitor supplies the load on its own.

Reverse voltage on the diode

Simplified, no leakage
Applying Volt-Second Balance, CCM

- The power switch turns off: $D$ conducts, $V_{out}$ "flies" back

$$V_{DS,off} = V_{in} + \frac{V_{out}}{N} = V_{in} + V_r$$

$$\frac{V_{out}}{V_{in}} = \frac{Nt_{on}}{t_{off}} = \frac{NDT_{sw}}{(1-D)T_{sw}} = \frac{ND}{1-D}$$

dc transfer function in CCM
Applying Volt-Second Balance, DCM

In DCM, when $L_p$ is fully depleted $D$ opens: $V_{out}$ reflection is lost.

\[
V_{DS,off} = V_{in}
\]

\[
\frac{V_{out}}{V_{in}} = ND \sqrt{\frac{R_{\text{load}}}{2L_p F_{sw}}}
\]

dc transfer function in DCM
Flyback, Typical Waveforms

- Below is a simple flyback converter, without parasitics

- It will run open loop for simplicity, $V_{out} \approx 8\ V$

No parasitics
Flyback, Typical Waveforms, CCM

CCM flyback – no parasitics

Input current
Inductor current
Diode blocks
Drain voltage
Output voltage
Output capacitor supplies the load
Diode current

Diode current

Output capacitor refueling

Output capacitor supplies the load

Diode current

CCM flyback – no parasitics
Flyback, Typical Waveforms, DCM

- **Input current**
- **Inductor current**
- **Drain voltage**
- **Output voltage**
- **Diode current**

DCM flyback – no parasitics
Energy Transfer in CCM and DCM

- The primary inductance, $L_p$, stores and releases energy

\[
E_{L_p, \text{valley}} = \frac{1}{2} L_p I_{\text{valley}}^2
\]
Initially stored energy

\[
E_{L_p, \text{peak}} = \frac{1}{2} L_p I_{\text{peak}}^2
\]
Stored energy at $t_{\text{on}}$

\[
E_{L_p, \text{accu}} = \frac{1}{2} L_p I_{\text{peak}}^2 - \frac{1}{2} L_p I_{\text{valley}}^2 = \frac{1}{2} L_p \left( I_{\text{peak}}^2 - I_{\text{valley}}^2 \right)
\]
Accumulated energy at $T_{\text{sw}}$

- Power (W) is energy (J) averaged over time (s):

\[
P_{\text{out}} = \frac{1}{2} \left( I_{\text{peak}}^2 - I_{\text{valley}}^2 \right) L_p F_{\text{sw}} \eta
\]
Eta, the efficiency

CCM

\[
P_{\text{out}} = \frac{1}{2} I_{\text{peak}}^2 L_p F_{\text{sw}} \eta
\]
DCM, $I_{\text{valley}} = 0$
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Considering Parasitic Elements

- The transformer and the MOSFET include parasitics.

![Circuit Diagram]

With parasitics:

- Lp = 2.2m
- k = 0.02
- Leak = Lp * k

Parameters:
- Lp = 2.2m
- k = 0.02
- Leak = Lp * k

\[ \text{Leak} = L_p \times k \]
Considering Parasitic Elements, CCM

- Input current
- Inductor current
- Drain voltage
- Output voltage
- Diode current

CCM mode – with parasitics
Considering Parasitic Elements, DCM

Input current
Inductor current
Drain voltage
Output voltage
Diode current

DCM mode – with parasitics
Who Are the Stray Elements?

- The study of the drain node reveals a \( LC \) network

\[ V_{\text{bulk}} \]

- \( L_p \) primary inductor
- \( l_{\text{leak}} \) leakage inductor
- \( C_{\text{oss}} \) output capacitance
The MOSFET $C_{OSS}$ is a Non-Linear Device

- The capacitor value changes with its bias voltage

\[ C_{OSS} (V_{DS}) = \frac{C_{D0}}{\sqrt{1 + \frac{V_{DS}}{V_0}}} \]

$C_{D0}$ is the cap. for $V_{DS} = V_0$

- As bias affects the capacitor value:

\[ W = \frac{1}{2} C_{OSS} V_{DS}^2 \]
As the Voltage Decreases, $C_{OSS}$ Value Changes

- The brutal discharge generates switching losses

$$I_C(t) = C \frac{dV_C(t)}{dt} \quad W = \int_0^t I_C(t) V_C(t) \cdot dt$$

$$W = \int_0^t C \frac{dV_{DS}(t)}{dt} V_{DS}(t) \cdot dt = \int_0^{V_{DS}} C(V_{DS}) V_{DS} \cdot dV_{DS}$$

$$C_{OSS}(V_{DS}) \approx \frac{C_{D0} \sqrt{V_0}}{\sqrt{V_{DS}}} \quad W = \frac{2}{3} V_{DS}^{3/2} C_{D0} \sqrt{V_0}$$

- The energy lost is smaller with the non-linear variation!

At turn-off
Using the Raw $C_{\text{OSS}}$ is an … Overkill

- Re-compute the capacitor from the MOSFET data-sheet

<table>
<thead>
<tr>
<th>Input Capacitance</th>
<th>$C_{\text{iss}}$</th>
<th>—</th>
<th>1300</th>
<th>—</th>
<th>pF</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reverse Transfer</td>
<td>$C_{\text{rss}}$</td>
<td>—</td>
<td>130</td>
<td>—</td>
<td></td>
</tr>
<tr>
<td>Capacitance</td>
<td></td>
<td>—</td>
<td>400</td>
<td>—</td>
<td></td>
</tr>
<tr>
<td>Output Capacitance</td>
<td>$C_{\text{oss}}$</td>
<td>—</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- The classical equation gives:

$$W = \frac{1}{2} C_{\text{OSS}} V_{DS}^2 = 0.5 \times 400 \times 100^2 = 2 \, \mu J \quad \text{or} \quad 200 \, \text{mW} @ \, 100 \, \text{kHz}$$

- The updated equation gives:

$$W = \frac{2}{3} V_{DS}^{3/2} C_{D0} \sqrt{V_0} = \frac{2}{3} \times 100^{3/2} \times 400 \times \sqrt{10} = 843 \, \text{nJ}$$

or $84 \, \text{mW} @ \, 100 \, \text{kHz} = 58\%$ reduction
The Leakage Inductance

- The coupling in a transformer is not perfect

- Some induction lines couple in the air: leakage flux
An Equivalent Transformer Model

- For a two-winding transformer, the model is simple:
  - Two leakage inductors
  - One magnetizing inductor

- This is commonly known as the "PI" model
The Transformer Scales the Primary Current

- In a perfect transformer, we have:

\[ I_{\text{sec}} = \frac{I_p}{N} \]

- The turns ratio is usually normalized to the primary

\[ N_p : N_s \quad \text{Divide by } N_p \quad \frac{N_p}{N_p} : \frac{N_s}{N_p} \quad \rightarrow \quad 1 : N \]

\[ N_p = 100 \]
\[ N_s = 25 \]

\[ 1 : 0.25 \]
\[ 1 \mid 250 \text{m} \]
The Leakage Term also Stores Energy

- At turn-on, the primary current flows in both $l_{\text{leak}}$ and $L_p$

\[
S_{on} = \frac{V_{in}}{L_p + l_{\text{leak}}}
\]

\[
N = 1
\]

- During the on-time, both $L_p$ and $l_{\text{leak}}$ store energy

\[
W_{\text{leak}} = \frac{1}{2} l_{\text{leak}} I_p^2
\]
Where does the Current Flow?

- At turn-off, the energy stored in $L_p$ is dumped in the output cap.

- The leakage inductor current fills up the drain lump capacitor.

\[
I_{\text{leak}}(t) + I_{L_p}(t) - I_{\text{leak}}(t) = V_{\text{out}}(t)
\]
Watch out for the Maximum Excursion!

- As the diode conducts, $V_{out}$ reflects over $L_p$

$$V_{DS,max} = V_{in} + \left( \frac{V_{out} + V_f}{N} \right) + I_{peak} \sqrt{\frac{l_{leak}}{C_{lump}}}$$

- The voltage on the drain increases dangerously!
We Need to Clamp that Voltage

- MOSFETs have a voltage limit they can fly up to: $BV_{DSS}$
- A clamping circuit has been installed to respect a margin

\[ BV_{DSS} = 600 \text{ V} \]
Resetting the Leakage Inductance

- Because of the clamp action, a voltage appears across $l_{\text{leak}}$

$$V_{\text{leak}} = V_{\text{clamp}} - (V_{\text{out}} + V_f)$$

- This voltage forces a reset of the leakage inductance
Do we Need a Quick Reset?

- When current flows in $I_{\text{leak}}$, it is diverted from the secondary

$$I_{L_p}(t) - I_{\text{leak}}(t)$$

At the switch opening:

$$I_{L_p}(t) = I_{\text{leak}}(t)$$

$$I_{\text{sec}}(t) = 0$$

- The leakage current delays the occurrence of the sec. current
$I_{\text{leak}}$ Delays the Secondary Current

- The leakage inductor reduces the peak secondary current

![Graph showing the relationship between primary and secondary currents](image)

- The "stolen" energy is dissipated as heat in the clamping network
- Less energy is transmitted to the secondary side
A Reduced Secondary-Side Current

- We can calculate the leakage inductor reset time $\Delta t$

$$S_{leak} = \frac{V_{clamp} - (V_{out} + V_f)}{I_{leak}}$$

$$\Delta t = \frac{I_{peak}}{S_{leak}} = \frac{l_{leak} I_{peak}}{V_{clamp} - (V_{out} + V_f)}$$

$$N \neq 1 \quad \Delta t = \frac{I_{peak}}{S_{leak}} = \frac{N l_{leak} I_{peak}}{N V_{clamp} - (V_{out} + V_f)}$$

$$I_{sec} = \frac{I_{peak}}{N} - S_{sec} \Delta t = \frac{I_{peak}}{N} \left(1 - \frac{l_{leak} L_p}{N V_{clamp}} \left(\frac{1}{V_{out} + V_f} - 1\right)\right)$$

$$\frac{l_{leak}}{L_p} = 1.8\%, \quad \frac{N V_{clamp}}{V_{out} + V_f} = 1.5$$

$$I_{sec} = \frac{I_{peak}}{N} - 3.6\%$$
Typical Example Simulation Results

- Primary current
- Leakage inductor current
- Sec. current
- Drain voltage

- $I_{\text{peak}} = 236 \text{ mA}$
- $I'_\text{peak} = 210 \text{ mA}$
- $\Delta t = 480 \text{ ns}$
- $I_{\text{peak}} = 2.1 \text{ A}$
- $11\%$ decrease!
A Ringing Appears as the Diode Blocks

As the clamp diode blocks, the drain returns to

\[ V_{in} + \frac{V_{out} + V_f}{N} \]

An oscillation takes place

\[ V_{in} + V_{clamp} + V_r \]

\[ I_{leak}(t) = 0 \]

\[ \Delta t \]

\[ f = \frac{1}{2\pi \sqrt{l_{leak} C_{lump}}} \]
The Primary Inductor also Rings in DCM

- When \( L_p \) is reset, the capacitor voltage returns to \( V_{\text{in}} \).

An oscillation takes place

\[
f = \frac{1}{2\pi \sqrt{(L_p + l_{\text{leak}})C_{\text{lump}}}}
\]
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How these Parasitics Affect your Design?

- The leakage inductor induces a large spike at turn-off
- This voltage excursion must be kept under control

![Graph showing BV_DSS and V_{clamp}](image)

- The lump capacitor on the drain brings switching losses
- Is there a way to switch on again when discharged?

Asynchronous switching
- Fixed frequency
  - $V_{DS} > V_{in}$

Synchronous switching
- Variable frequency
  - $V_{DS} \ll V_{in}$
Protecting the Power MOSFET

- A vertical MOSFET features a buried parasitic NPN transistor
- The collector-base junction of this transistor forms the body-diode
- This « diode » can accept to avalanche in certain conditions
- Do NOT use this diode as a Transient Voltage Suppressor

✓ Adopt a safety coefficient $k_D$ when choosing the maximum $V_{DS}(t)$
✓ 15% derating is usually selected

$k_D = 0.85$

$BV_{DSS} \times k_D = 600 \times 0.85 = 510\, \text{V}$

$V_{clamp} = BV_{DSS} \times k_D - V_{os} - V_{in} = 115\, \text{V}$

Take $V_{os}$ around $15 - 20\, \text{V}$
Inclusion of a Safety Margin

- The voltage on the drain swings up to $V_{\text{clamp}}$

$BV_{DSS} = 600$ V

$V_{\text{clamp}}$  

$V_{os}$  

$V_{in}$  

$V_{DS}(t)$

100 V / div

Safety margin

- Test at start-up and in short-circuit

$V_{out} = $ nominal  
$I_{out} = $ max  
$V_{in} = $ max

- Capture this waveform in worst-case conditions
The Clamp Circuit Overshoots

- The clamp diode forward transit time delays the clamping action

\[ V_{os} = 14 \, \text{V} \]

- This spike can be lethal to the power MOSFET
Do not Reflect too Much Voltage

- The reflected voltage affects the power dissipation in the clamp

\[ P_{\text{clamp,avg}} = \frac{1}{2} F_{\text{sw}} L_{\text{leak}} I_{\text{peak}}^2 \left( \frac{k_c}{k_c - 1} \right) \]

\[ k_c = \frac{V_{\text{clamp}}}{V_r} \]

- If \( V_{\text{clamp}} \) is too close to \( V_r \), dissipation occurs \( \rightarrow k_c = 1.3 \) to 2

![Graph showing the relationship between \( P_{\text{clamp}} \) and \( k_c \)]
Compute the Transformer Turns Ratio

- The turns ratio affects the reflected voltage...

\[ V_{\text{clamp}} \geq k_c \frac{(V_{\text{out}} + V_f)}{N} \]

\[ N \geq \frac{k_c (V_{\text{out}} + V_f)}{V_{\text{clamp}}} \]

- But also the Peak Inverse Voltage of the secondary diode

\[ \text{PIV} = V_{\text{in}}N + V_{\text{out}} \]

Choose a 100% derating factor

If \( \text{PIV} = 100 \text{ V} \) Then \( \text{BV} = 200 \text{ V} \)

- Always check the margins are not violated in any operating modes
Select the Clamp Passive Elements

- The clamp resistor depends on the maximum peak current

\[ R_{clp} = \frac{2V_{clamp}}{F_{sw}I_{leak}I_{peak}^2} \left[ V_{clamp} - \frac{(V_{out} + V_f)}{N} \right] \]

\[ C_{clp} = \frac{V_{clamp}}{R_{clp} F_{sw} \Delta V} \]

\[ I_{peak,max} = \frac{V_{sense,max}}{R_{sense}} + \frac{V_{in,max}}{L_p} t_{prop} \]

Worst-case value

- Watch for the peak current overshoot in fault!
Clamp Current is Smaller

- Lump capacitance charge at turn off depletes the leakage energy

\[ \Delta I = 234 \text{ mA} \]

\[ \frac{0.234}{1.84} \times 100 = 13\% \]

\[ 1.13^2 = 1.28 \]

Power is reduced by 28%
The Leakage Inductor Rings

- This ringing can be of high frequency and is radiated-EMI rich

- It can also forward-bias the MOSFET body diode
- Damp it!
Fighting Parasitic Ringing – part I

- The installed resistor reduces the ringing on the drain

\[ Q = \frac{\omega_0 l_{\text{leak}}}{R_{\text{damp}}} = 1 \quad \text{and} \quad Z_{l_{\text{leak}}} @ f_0 = R_{\text{damp}} \]
Fighting Parasitic Ringing – part II

If the series resistor is not enough, install a damper

1. Measure the ringing: $f_0$

2. Evaluate leakage impedance at $f_0$

\[ Z_{leak} = 2\pi l_{leak} f_0 \]

3. Make $R_{damp} = Z_{leak}$

4. Try $C_{damp} = \frac{1}{2\pi f_0 R}$

5. Tweak for power dissipation

Ray Ridley – Snubber design procedure
Effects brought by clamping action

\[ V_{\text{peak}} = 510 \, V \]

\[ F_{\text{clp}} = 2.08 \, \text{MHz} \]

No damper – zoom

\[ V_{\text{DS}}(t) \]

\[ V_{\text{peak}} = 452 \, V \]

\[ R_{\text{damp}} = 290 \, \Omega - C_{\text{damp}} = 220 \, \text{pF} \]

No damper

Can forward bias the body diode

\[ V_{\text{peak}} = 494 \, V \]

\[ R_{\text{damp}} = 290 \, \Omega - C_{\text{damp}} = 50 \, \text{pF} \]
What Diode to Select for the Clamp?

- A fast diode is a must: MUR160 is good fit

Can a simple 1N4007 be used in a RCD clamping network?
- The answer is yes for low power applications (below 20 W)
- The long recovery time naturally damps the leakage inductor
Be Sure the Clamp Level does not Runaway

- Watch-out for clamp voltage variations, at start-up or in short-circuit
- The main problem comes from the propagation delay!
Check the Clamp Voltage Variations

No design margin!

- **Drain voltage**
- **Clamp voltage**
- **Sense voltage**
- **Output voltage**

Worst case
A Zener or TVS to Hard Clamp the Voltage

- TVS do not suffer from voltage runaways in fault conditions

\[ P_{TVS} = \frac{1}{2} F_{sw} l_{\text{leak}} I_{\text{peak}}^2 \frac{V_z}{V_z - \left( \frac{V_{out} + V_f}{N} \right)} \]

- The TVS improves the efficiency in standby but degrades EMI
  - It costs around 5 cents…
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What Control Scheme?

- Two control scheme coexist, current-mode and voltage-mode

Voltage-mode?

Current-mode?

Operating waveforms are identical

Voltage-mode?

Current-mode?

Ac-transfer functions differ
Voltage-Mode Control

- Voltage mode uses a ramp to generate the duty-ratio
- The error voltage directly adjusts the duty-ratio
Voltage-Mode Control

PROs

- Does not need the inductor current information
  - Can go to very small duty-ratio
- CCM operation without sub-harmonic instabilities
  - No need for slope compensation, current limit unaffected

CONs

- No inherent input line feedforward (weak audio susceptibility)
  - Cannot use small bulk capacitor, bad ripple rejection
- 2nd-order system in CCM: mode transition can be a problem
- Limited integrated circuit offer
Peak-Current-Mode Control

- Current mode uses the inductor current information as a ramp
- The error voltage adjusts the inductor peak current
- The duty-ratio is indirectly controlled
Peak-Current-Mode Control

**PROs**

- Inherent pulse-by-pulse current limitation
- Natural input line rejection
- Mode transition DCM to CCM is easy
  - Converter remains a 1\textsuperscript{st}-order system at low frequency
- Widest offer on the market: a really popular technique!

**CONs**

- Leading Edge Blanking limits the minimum duty-ratio
- Requires slope compensation against sub-harmonic oscillations
  - Additional ramp affects the available maximum peak current
- Current sense can sometimes be a problem (floating sense)
A Dirty Inductor Current Signal

- The inductor current is sensed with a resistor, a transformer...
- This information is affected by parasitics: false tripping possible!

![Graph showing the inductor current signal with potential false tripping points](image)
The LEB Cleanses the Signal

- A circuit blinds the controller at turn-on for a small time (≈250 ns)
- It conveys the signal afterwards: Leading Edge Blanking

![Diagram of LEB mechanism]

\[ V_{\text{bulk}} \]

\[ \text{PWM reset} \]

\[ t_{\text{LEB}} \]

\[ \text{DRV} \]

\[ R_{\text{sense}} \]

\[ V_{\text{sense}}(t) \]

Clean edges
It Limits the Minimum Duty-Ratio

- During the LEB duration, the controller is completely blind!
- In output winding short-circuits, failures are likely to occur

![Diagram showing waveforms and equations related to LEB duration and duty-ratio limitations.](image-url)
If the Primary Inductor is too Low...

- In short-circuit situations, you reflect the diode forward drop

\[ V_f = \frac{V_{bulk}}{N} \]

- If you hit the minimum on-time, you cannot limit the current!
The Primary Current Runs out of Control

- The current current climbs cycle by cycle until smoke appears!

- Maximum theoretical peak value, 5 A
- The current climbs-up to 9 A!!

- Demagnetization too weak

- Minimum \( t_{on} \)

- \( V_{sense}(t) \)

- First design…

- Chris Basso
Sub-Harmonic Oscillations

- Ac analysis shows a first-order system at $f_c << \frac{F_{sw}}{2}$
  - No $LC$ peaking anymore as in CCM voltage mode
  - But a subharmonic peaking at $\frac{F_{sw}}{2}$ now appears

![Graph](image)

Flyback power stage in CCM
Instability Depends on Duty-Ratio

- The condition for instability is: CCM operation + duty-ratio > 50%

\[ I_{peak} = a + S_1 \Delta t \]
\[ b = I_{peak} - S_2 \Delta t \]

Solving for \( \Delta t \):

\[ \frac{I_{peak} - a}{S_1} = \frac{I_{peak} - b}{S_2} \]

\[ S_2 \quad \text{and} \quad S_1 \]

\[ \frac{S_2}{S_1} = \frac{d}{d'} \]

\[ \Delta I_L (nT_{sw}) = \Delta I_L (0) \left( -\frac{d}{d'} \right)^n \]
Instability Depends on Duty-Ratio

- With a duty-ratio below 50%, perturbation naturally dies out …

\[ \Delta I_L(nT_{SW}) = \Delta I_L(0) \left( -\frac{d}{d'} \right)^n \]

- Duty-ratio < 50%

- Duty-ratio > 50%

Asymptotically stable

Asymptotically unstable
The Cure is in the Ramp

Injecting a ramp on the feedback signal, damping is obtained:

\[ \Delta I_L(n T_{sw}) = \Delta I_L(0) \left[ \frac{1 - \frac{S_a}{S_2}}{d' + \frac{S_a}{S_2}} \right]^n = \Delta I_L(0)(-a)^n \]

- Must stay below 1
- Up to \( d = 100\% \)
- \( 0 + \left| \frac{1 - \frac{S_a}{S_2}}{\frac{S_a}{S_2}} \right| < 1 \)
- \( S_a > 50\% S_2 \)
A Model to Simulate a Flyback Converter

- A SPICE model can predict subharmonic instabilities

```
parameters

Vout=19
Soff=(Vout/(N*Lp))*Ri

N=250m
Fsw=65k
Lp=350u
Ri=250m
A=0.5
Se=A*Soff
```
Simulation Results of the CCM Flyback

- As ramp is injected, the double-pole $Q$ is damped
- Injecting more ramp turns the converter into voltage-mode

![Graph 1](image1.png)

$$|H(s)| \quad S_a = 50\%S_2$$

![Graph 2](image2.png)

$$\angle H(s) \quad S_a = 50\%S_2$$
Modern Circuits Include Slope Compensation

- A simple resistor in series with current sense resistor does the job

![Circuit Diagram]

- Adjust the resistor to set the ramp to any level

NCP1250
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The most popular modulation strategy is trailing-edge modulation.

Leading-edge modulation often appears in post-regulators.
Fixed Frequency Operation

- The vast majority of converters use fixed-frequency operation
  - Switching losses depend on frequency: high frequency, high losses!
  - Capacitive losses are a brake to efficiency improvement
  - CCM operation induces high losses on the secondary diode
  - Potential shoot-through hampers synchronous rectification
  - The Right Half-Plane Zero severely limits the available bandwidth

![Graphs showing noise and losses in the input and output currents and voltages.](image)
The Right-Half-Plane Zero

- In a CCM flyback, $I_{out}$ is delivered during the off-time:

$$I_d(t)$$

- If $D$ brutally increases, $D'$ reduces and $I_{out}$ drops!
- What matters is the inductor current slew-rate

$$\left\langle \frac{dv_L(t)}{dt} \right\rangle$$
Processing the Output Power Demand

- If $i_L(t)$ can rapidly change, $I_{out}$ increases when $D$ goes up

![Graph showing the relationship between $d(t)$, $v_{out(t)}$, $i_L(t)$, and $i_{out(t)}$.]
Failing to Increase the Current in Time

- If $i_L(t)$ is limited because of a big $L_p$, $I_{out}$ drops when $D$ increases.

![Graph showing $d(t)$, $v_{out}(t)$, $i_L(t)$, and $i_{out}(t)$ with $V_{out}$ drops at $d = 59\%$ and $I_{out}$ drops at $d = 58.3\%$.]
The RHPZ is a Positive Root

- Small-signal equations can help us to formalize it

\[
\frac{v_{out}(s)}{d(s)} = G_0 \left( 1 + \frac{s}{\omega_{z_1}} \right) \left( 1 - \frac{s}{\omega_{z_2}} \right) \frac{1}{1 + \frac{s}{Q\omega_0} + \left( \frac{s}{\omega_0} \right)^2}
\]

Voltage mode

\[
\frac{\hat{v}_{out}(s)}{\hat{v}_c(s)} = G_0 \left( 1 + \frac{s}{\omega_{z_2}} \right) \left( 1 - \frac{s}{\omega_{z_3}} \right) \frac{1}{D(s)}
\]

Current mode

\[
\omega_{z_2} = \frac{R_{load} D^2}{N^2 DL}
\]

- Voltage mode or current mode, the RHPZ remains the same
Simulating the RHPZ

- To limit the effects of the RHPZ, limit the duty ratio slew-rate.
- Choose a crossover frequency equal to 20-30% of RHPZ position.
  - A simple RHPZ can be easily simulated:

\[
V_{\text{out}}(s) = V_{\text{in}}(s) - \frac{R_1}{1 + \frac{s}{sC_1}} = V_{\text{in}}(s) \left(1 - \frac{s}{\omega_0}\right)
\]
A Zero Producing a Phase Lag

- With a RHPZ we have a boost in gain but a lag in phase!

\[ G(s) = 1 + \frac{s}{\omega_0} \]

- LHPZ

\[ |V_{out}(s)| \]

- RHPZ

\[ \arg V_{out}(s) = -90^\circ \]
Is There a RHPZ in DCM?

- A RHPZ also exists in DCM boost, buck-boost converters…

When \( D_1 \) increases, \([D_1, D_2]\) stays constant but \( D_3 \) shrinks.
Is There a RHPZ in DCM?

- The triangle is simply shifted to the right by \( \hat{d}_1 \)

\[
i_d(t)
\]

- The refueling time of the capacitor is delayed and a drop occurs
Is There a RHPZ in DCM?

- If $D$ increases, the diode current is delayed by $\hat{d}_1$.
A Large-Signal Model is Available

- Averaged models can predict the DCM RHPZ

\[ \hat{v}_{out}(s) = H_d \left(1 + s/s_{z1}\right) \left(1 - s/s_{z2}\right) \]

\[ \hat{d}(s) = \frac{1}{1 + s/s_{p1}} \left(1 + s/s_{p2}\right) \]

\[ s_{z1} = \frac{1}{C_{out} R_{ESR}} \quad s_{z2} = \frac{R_{load}}{M^2 L} \]

\[ s_{p1} = \frac{2M - 1}{M - 1} \quad s_{p2} = 2F_{sw} \left(1 - 1/M\right)^2 \]

\[ H_d = \frac{2V_{out}}{D} \left(\frac{M - 1}{2M - 1}\right) \]

Merci Vatché!
The Model Predicts it!

Averaged models can predict the DCM RHPZ

$H_d = 28.75 \, dB$

$f_{z_1} = 1.06 \, kHz$

$f_{z_2} = 141 \, kHz$

$f_{p_1} = 4.2 \, Hz$

$f_{p_2} = 47.1 \, kHz$
Going to Variable Frequency

- More converters are using variable-frequency operation
- This is known as Quasi-Square Wave Resonant mode: QR
  - Valley switching ensures extremely low capacitive losses
  - DCM operation saves losses on the secondary diode
  - Easier synchronous rectification
  - The Right Half-Plane Zero is pushed to high frequencies
What is the Principle of Operation?

- The drain–source signal is made of peaks and valleys
- A valley presence means:
  - The drain is at a minimum level, capacitors are naturally discharged
  - The converter is operating in the discontinuous conduction mode
A QR Circuit Does not Need a Clock

- The system is a self-oscillating current-mode converter

![Circuit Diagram]
A Winding is Used to Detect Core Reset

- When the flux returns to zero, the aux. voltage drops
- Discontinuous Mode is always maintained

\[ V_{\text{aux}} = -N \frac{d\phi}{dt} \]

When the flux returns to zero, the aux. voltage drops. Discontinuous Mode is always maintained.
The Frequency Linearly Changes

- As the peak current and the on-slope vary, $T_{sw}$ changes

$$i_{L_p}(t) \quad I_{peak,max}$$

- Excellent behavior in short-circuit conditions!

$$S_{on,HL} = \frac{V_{in,HL}}{L_p} \quad S_{on,LL} = \frac{V_{in,LL}}{L_p}$$

$$S_{off} = \frac{(V_{out} + V_f)}{NL_p}$$

**low** rms currents in the MOSFET (weak stress)
The Excursion Can be Quite Large

- In heavy load low-line conditions, $F_{sw}$ decreases
- In light-load and high-line operations, $F_{sw}$ can go very high

- EMI and switching losses are at stake as $F_{sw}$ goes up
- Standby power obviously suffers from this condition
In a Bounded System Discrete Jumps

- As the load gets lighter, the frequency goes to the sky
- Modern controllers fold the frequency back with a VCO
- Problem, the only places to re-start are valleys: discrete jumps
New Controllers Lock in the Valleys

- To prevent the noise, the NCP1380 locks the valley
- The current is allowed to move within a certain limit
- When it exceeds this limit, the controller selects a new valley
- As the load gets lighter, a VCO takes over and reduce $F_{sw}$
Course Agenda

- The Flyback Converter
- The Parasitic Elements
- How These Parasitics Affect your Design?
- Current-Mode is the Most Popular Scheme
- Fixed or Variable Frequency?
- More Power than Needed
- The Frequency Response
- Compensating With the TL431
What is The Problem?

- A converter is designed to operate on wide mains – 85 to 265 V rms
- It can deliver a maximum power before protection trips
  - The maximum power delivered at high line is larger than that at low line

85 V rms to 265 V rms

Increase load until protection trip.
What Does the Standard Say?

- There is a test called Limited Power Source, LPS
- The maximum power the converter can deliver must be clamped
- If clamped, the manufacturer can use inferior fire proofing materials

<table>
<thead>
<tr>
<th>Output Voltage $V_{out}$ (V)</th>
<th>Output Current $I_{out}$ (A)</th>
<th>Apparent Power $S$ (VA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{rms}$</td>
<td>$V_{dc}$</td>
<td>$\leq 8$</td>
</tr>
<tr>
<td>$\leq 20$</td>
<td>$\leq 20$</td>
<td></td>
</tr>
<tr>
<td>$20 &lt; V_{out} \leq 30$</td>
<td>$20 &lt; V_{out} \leq 30$</td>
<td>$\leq 8$</td>
</tr>
<tr>
<td>-</td>
<td>$20 &lt; V_{out} \leq 60$</td>
<td>$\leq 150/V_{out}$</td>
</tr>
</tbody>
</table>

19-V adapter, $I_{out,\text{max}} = 5$ A

IEC950 safety standard
Why the Power Runs Away in a Flyback?

- The inductor current slope increases at high line.
- The controller takes time to react to an overcurrent situation.
- The inductor current keeps growing until the MOSFET turns off.
- The overshoot is larger at higher slopes (High $V_{in}$).

$\Delta I_{\text{peak,LL}}$ depends on drive capability and MOSFET $Q_G$.

\[ I_{\text{peak}} = I_{\text{peak,max}} + \frac{V_{\text{in,max}}}{L_p} t_{\text{prop}} \]

\[ S = \frac{V_{\text{in}}}{L_p} \]

\[ I_{L_p}(t) \]

\[ CS_{\text{out}}(t) \]

\[ V_{GS}(t) \]

\[ t_{\text{del}} \]

\[ t_{\text{prop}} \]
The Effect in a DCM Converter

A flyback converter operated in DCM obeys the formula:

\[
P_{\text{out}} = \frac{1}{2} L_p I_{\text{peak, max}}^2 F_{\text{sw}} \eta
\]

- \( P_{\text{out}} \): Output power
- \( L_p \): Primary inductor
- \( I_{\text{peak, max}} \): Max. peak current in fault
- \( F_{\text{sw}} \): Switching frequency
- \( \eta \): Converter efficiency

As \( L_p \) and \( F_{\text{sw}} \) are fixed, \( I_{\text{peak, max}} \) changes with line input.

\[
I_{\text{peak, max, LL}} = \frac{V_{\text{sense}}}{R_{\text{sense}}} + \frac{V_{\text{in, LL}}}{L_p} t_{\text{prop}}
\]

Low line

\[
I_{\text{peak, max, HL}} = \frac{V_{\text{sense}}}{R_{\text{sense}}} + \frac{V_{\text{in, HL}}}{L_p} t_{\text{prop}}
\]

High line

\[
\frac{\Delta I_{\text{peak}}}{I_{\text{peak, max, HL}}} = \frac{V_{\text{in, HL}} - V_{\text{in, LL}}}{L_p V_{\text{sense}}} \frac{t_{\text{prop}}}{R_{\text{sense}}} + V_{\text{in, LL}}
\]

A 13.5% overshoot translates in a 28% power increase

\((\eta \text{ is considered constant over the range})\)
The Power Increases at High Line

- $L_p = 250 \, \mu\text{H}$, $V_{\text{sense}} = 1 \, \text{V}$, $t_{\text{prop}} = 350 \, \text{ns}$, $V_{\text{in,LL}} = 120$, $V_{\text{in,HL}} = 370 \, \text{V}$, $R_{\text{sense}} = 0.33 \, \Omega$, $F_{\text{sw}} = 65 \, \text{kHz}$

In this example, the converter stays DCM on the whole range.
How to Compensate the Runaway?

- How do we compensate this excess of power?
  - we reduce the maximum peak current at high line
  - this is called Over Power Protection – OPP

- How to calculate the compensated high-line current?
  - Equate low-line power with high-line power and solve for $I_{\text{peak}}$

\[
P_{\text{out},\text{max},HL} = \frac{1}{2} L_p I_{\text{peak,max},HL}^2 F_{\text{sw}} \eta_{HL}
\]

Solve for $I_{\text{peak}}$
Reducing the Peak Current

- The final inductor peak current must equal:

\[ I_{\text{peak, max, HL}} = \sqrt{\frac{2P_{\text{out, max, LL}}}{L_p F_{\text{sw}} \eta_{\text{HL}}}} \]

- The compensated setpoint must subtract the prop. delay:

\[ \frac{V_{\text{sense}}}{R_{\text{sense}}} = I_{\text{peak, max, HL}} - \frac{V_{\text{in, HL}}}{L_p} t_{\text{prop}} \]

- The amplitude of the sensed voltage must reduce by:

\[ \Delta V = V_{\text{sense}} - \left( I_{\text{peak, max, HL}} - \frac{V_{\text{in, HL}}}{L_p} t_{\text{prop}} \right) R_{\text{sense}} \]
For What Final Result?

Thanks to the OPP, the power stays under control

\[ P_{out} = 4W \]
The CCM Case is a Different Picture

- In DCM, the valley current is zero, the stored energy is:

\[ E = \frac{1}{2} L_p I_{\text{peak, max}}^2 \]

- The peak current runaway, alone, affects the transmitted power.

- In CCM, the valley current changes the formula:

\[ E = \frac{1}{2} L_p \left( I_{\text{peak, max}}^2 - I_{\text{valley}}^2 \right) \]
The Converter Changes its Operating Mode

- In fault mode, the converter operates in deep CCM at low line
- As the input voltage increases, the valley current decreases

\[ I_{L_p}(t) \]

- For Low line:
  \[ I_{p,\text{max,LL}} = \frac{V_{\text{in,min}}}{L_p} \]
  \[ I_{p,\text{valley,LL}} = \frac{(V_{\text{out}} + V_f)}{N L_p} \]

- For High line:
  \[ I_{p,\text{max,HL}} = \frac{V_{\text{in,max}}}{L_p} \]
  \[ I_{p,\text{valley,HL}} = \frac{(V_{\text{out}} + V_f)}{N L_p} \]

\[ E_{HL} > E_{LL} \]
Computing the Transmitted Power in CCM

First, we write the $t_{on}$ and $t_{off}$ equations in CCM

\[ I_{LP}(t) \]

\[ I_{\text{peak}} \]

\[ I_{\text{valley}} \]

\[ t_{on} \]

\[ t_{off} \]

\[ T_{sw} \]

\[ I_{\text{peak}} = I_{\text{valley}} + \frac{V_{in}}{L_p} t_{on} \]  \hspace{2cm} \[ I_{\text{valley}} = I_{\text{peak}} - \frac{(V_{out} + V_f)}{NL_p} t_{off} \]  \hspace{2cm} \[ T_{sw} = t_{on} + t_{off} \]  

\(1\) \hspace{2cm} \(2\) \hspace{2cm} \(3\)
Solving for the Valley Current

- By combining the 3 equations, we have:
  \[ t_{on} = \frac{L_p (I_{peak} - I_{valley})}{V_{in}} \]
  \[ t_{off} = T_{sw} - t_{on} = T_{sw} - \frac{L_p (I_{peak} - I_{valley})}{V_{in}} \]

- Replace \( t_{off} \) in (2):
  \[ I_{valley} = I_{peak} - \frac{(V_f + V_{out})(I_{valley}L_p - I_{peak}L_p + T_{sw}V_{in})}{L_p NV_{in}} \]

- Solve for \( I_{valley} \):
  \[ I_{valley} = I_{peak} - \frac{T_{sw}V_{in} (V_f + V_{out})}{L_p (V_f + V_{out} + NV_{in})} \]
  \[ \Delta I_L = I_{peak} - I_{valley} \to LL \text{ or } HL \]
  \[ \Delta I_L = \frac{T_{sw}V_{in} (V_f + V_{out})}{L_p (V_f + V_{out} + NV_{in})} \]

- Max fault current
  \[ I_{peak,\text{max}} = \frac{V_{sense}}{R_{sense}} + \frac{V_{in}}{L_p} t_{prop} \]
Identifying the Operating Mode

- Having the ripple on hand, we can confirm the mode:

\[ t_{on} = \frac{\Delta I_L}{V_{in}} L_p \]
\[ t_{off} = \frac{N \Delta I_L}{(V_{out} + V_f)} L_p \]

- \( t_{on} + t_{off} = T_{sw} \) 
  - \( I_{valley} > 0 \) \( \rightarrow \) CCM
  - \( I_{valley} = 0 \) \( \rightarrow \) BCM

- \( t_{on} + t_{off} < T_{sw} \) 
  - \( DT = T_{sw} - t_{off} - t_{on} \) \( \rightarrow \) DCM
Evaluating the Power in CCM

- \( L_p = 600 \, \mu H, \ V_{sense} = 1 \, V, \ t_{prop} = 350 \, \text{ns}, \ V_{in,LL} = 120, \ V_{in,HL} = 370 \, V, \ R_{sense} = 0.33 \, \Omega, \ F_{sw} = 65 \, \text{kHz} \)

\[
P_{max,LL} = \frac{1}{2} L_p \left( I_{peak,max,LL}^2 - I_{valley,LL}^2 \right) F_{sw} \eta_{LL} \approx 76 \, \text{W}
\]

\[
P_{max,HL} = \frac{1}{2} L_p \left( I_{peak,max,HL}^2 - I_{valley,HL}^2 \right) F_{sw} \eta_{HL} = 104 \, \text{W}
\]

\[\Delta P_{out} = 24 \, \text{W}\]
Reducing the Peak Current at High Line

- If we lower the peak at high line, the ripple remains the same.

\[ I_{L_p}(t) \]

\[ \Delta I_L \]

\[ \Delta I_{LCMP} \]

\[ t_{on}, t_{off}, T_{sw} \]

- We can re-write the flyback power formula to include the ripple:

\[ P_{max,HL} = \frac{1}{2} L_p \left( I_{peak,\text{max},HL}^2 - \left( I_{peak,\text{max},HL} - \Delta I_{L,HL} \right)^2 \right) F_{sw} \eta_{HL} \]

0 in DCM
We Want to Limit the High-Line Power

- We can force the high-line power to match that of low line

\[ P_{\text{max,LL}} = \frac{1}{2} L_p \left( I_{\text{peak, max, HL}}^2 - \left( I_{\text{peak, max, HL}} - \Delta I_{L, HL} \right)^2 \right) F_{\text{sw}} \eta_{HL} \]

- From there, we can extract the compensated peak current value

\[ I_{\text{peak, max, HL}} = \frac{F_{\text{sw}} L_p \eta_{HL} \Delta I_{L, HL}^2 + 2 P_{\text{max,LL}}}{2 F_{\text{sw}} L_p \eta_{HL} \Delta I_{L, HL}} \]

- As this is the new setpoint, prop. delay contribution must be removed

\[ \Delta V = V_{\text{sense}} - \left( I_{\text{peak, max, HL}} - \frac{V_{\text{in,HL}}}{L_p} t_{\text{prop}} \right) R_{\text{sense}} \]

- After compensation, the peak current setpoint at high line becomes

\[ I_{\text{peak, max, HL}} = \frac{V_{\text{sense}} - \Delta V}{R_{\text{sense}}} + \frac{V_{\text{in,HL}}}{L_p} t_{\text{prop}} \]
What is the Final Result?

- The high line power now respects the LPS limit

\[ \Delta P_{\text{out}} = 6 \, \text{W} \]
What Practical Solutions?

There are several possibilities to reduce the peak current:

1. Offset the current sense signal in the CS pin:

   \[ I(L_p) \]

   - easy to do
   - affects the no-load stand-by power
   - does not affect light-load efficiency

   • simple
   • affects the no-load stand-by power
   • does not affect light-load efficiency

2. Reduce the peak limit as \( V_{in} \) increases

   \[ I(L_p) \]

   • implemented at IC level
   • does not affect the no-load stand-by power
   • does not affect light-load efficiency
Build an Offset on the CS Pin

- This offset must be proportional to the input voltage

- Both options degrade light-load operation because of the offset
OPP Implementation in the NCP1250

- The NCP1250 implement a non-dissipative OPP circuitry

- The auxiliary swings to $-V_{in}$ and reduces the setpoint $\rightarrow$ OPP
Checking the Results

- Let us check on a real 19-V adapter built with the NCP1250

\[ L_p = 600 \, \mu\text{H}, \ V_{\text{sense}} = 1 \, \text{V}, \ t_{\text{prop}} = 350 \, \text{ns}, \ V_{\text{in,LL}} = 120, \ V_{\text{in,HL}} = 370 \, \text{V} \]
\[ R_{\text{sense}} = 0.33 \, \Omega, \ F_{\text{sw}} = 65 \, \text{kHz}, \ V_{\text{clamp}} = 90 \, \text{V}, \ l_l = 2.2 \, \mu\text{H}, \ N = 0.25 \]

- Without any OPP compensation, we have:

\[ I_{\text{out,max,LL}} = 4.1 \, \text{A} \quad I_{\text{out,max,HL}} = 5.7 \, \text{A} \]

- Once OPP has been implemented:

\[ P_{\text{out,LL}} \approx 72 \, \text{W} \quad \text{so} \quad I_{\text{out,LL}} = 3.8 \, \text{A} \quad \quad P_{\text{out,HL}} \approx 78 \, \text{W} \quad \text{so} \quad I_{\text{out,HL}} = 4.1 \, \text{A} \]
Course Agenda

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Small-Signal Analysis

- Loop instability is a common issue in production
- Due to time pressure, designers often use trial and error
  - no indication on design margins
  - offenders are ignored, robustness is at stake

\[
G(s) \rightarrow \begin{array}{c}
G(s) \\
\end{array} \rightarrow H(s)
\]

Understand and counteract their variations when building \(G(s)\)
There are Two Options

- Analytical analysis of the power stage:
  - best to see where the offenders are hidden (ESR, opto pole etc.)
  - equations are complex but literature abounds
    - transfer function are for DCM or CCM
    - difficult to predict transient response

- SPICE models:
  - easy-to-implement averaged models
  - can work in ac or transient mode
  - easily transition between CCM and DCM
    - do not explicitly disclose the position of poles and zeros

A measurement on the bench is mandatory, whatever you choose!
Analytical Analysis

- You must first characterize the "plant" transfer function
  - what are your power stage ac characteristics?

\[
V_{\text{ref}} / \alpha \xrightarrow{+} \varepsilon \xrightarrow{-} G(s) \xrightarrow{d(s)} H(s) \xrightarrow{+} V_{\text{out}}(s)
\]

\[
H(s) = \frac{V_{\text{out}}(s)}{v_c(s)}
\]

Current-mode control

\[
H(s) = \frac{V_{\text{out}}(s)}{d(s)}
\]

Voltage-mode control
How do we Stabilize a Converter?

- We need a high gain at dc for a low static error
- We want a sufficiently high crossover frequency for response speed
- Shape the compensator $G(s)$ to build phase and gain margins!

$$\phi_m = 92^\circ$$

$$f_c = 6.5 \text{ kHz}$$

$$\big|T(s)\big| = -67 \text{ dB}$$

$$GM = 67 \text{ dB}$$
How much phase margin to chose?

- a $Q$ factor of 0.5 (critical response) implies a $\varphi_m$ of 76°
- a 45° $\varphi_m$ corresponds to a $Q$ of 1.2: oscillatory response!

- phase margin depends on the needed response: fast, no overshoot…
- good practice is to shoot for 60° and make sure $\varphi_m$ always > 45°
What Compensator Types do we Need?

- There are basically 3 compensator types:
  - type 1, 1 pole at the origin, no phase boost
  - type 2, 1 pole at the origin, 1 zero, 1 pole. Phase boost up to 90°
  - type 3, 1 pole at the origin, 1 zero pair, 1 pole pair. Boost up to 180°
Fixed-Frequency Current-Mode

First, check the operating mode, CCM or DCM?

\[ L_{p,\text{crit}} = \frac{R_{\text{load}}}{2F_{\text{sw}}N^2} \left( \frac{V_{\text{in}}}{V_{\text{in}} + \frac{V_{\text{out}}}{N}} \right)^2 \]

\[ L_p > L_{p,\text{crit}}? \text{ Yes, CCM else DCM} \]

Assume CCM, compute the duty-ratio:

\[ D = \frac{V_{\text{out}}}{V_{\text{out}} + NV_{\text{in}}} \]

Compute \( M \) and \( \tau_L \):

\[ M = \frac{V_{\text{out}}}{NV_{\text{in}}} \quad \tau_L = \frac{2L_pN^2}{R_{\text{load}}T_{\text{sw}}} \]

Evaluate the dc gain and poles/zeros positions:

\[ G_0 = \frac{R_{\text{load}}}{R_{\text{sense}}G_{FB}N} \left( \frac{1}{(1 - D)^2} \right) + \frac{1}{\tau_L + 2M + 1} \]
Fixed-Frequency Current-Mode

- Compute the poles/zeros positions:
  \[ f_{z_1} = \frac{1}{2\pi R_{ESR} C_{out}} \quad f_{z_2} = \frac{(1-D)^2 R_{load}}{2\pi D L_p N^2} \quad f_{p_1} = \frac{\tau_L}{2\pi R_{load} C_{out}} \]

- Check the quality coefficient at \( F_{sw}/2 \)
  \[ S_n = \frac{V_{in}}{L_p} R_{sense} \quad S_e = (M_c - 1) S_n \quad Q_p = \frac{1}{\pi (M_c (1-D) - 0.5)} \]
  \( 1 = \) no compensation

- Apply to formula to plot the ac response:
  \[ H(s) \approx G_0 \frac{\left(1 + \frac{s}{\omega_{z_1}}\right)\left(1 - \frac{s}{\omega_{z_2}}\right)}{\left(1 + \frac{s}{\omega_{p_1}}\right)\left(1 + \frac{s}{\omega_{nQ_p}} + \frac{s^2}{\omega_n^2}\right)} \]
  \( 3^{rd} \) order \( M_c = 1 + \frac{S_e}{S_n} \quad \omega_n = \frac{\pi}{T_{sw}} \)
Fixed-Frequency Current-Mode

- Extract the magnitude and the argument definitions

\[
|H(f)| = 20 \log_{10} \left[ G_0 \sqrt{1 + \left( \frac{f}{f_{z1}} \right)^2} \sqrt{1 + \left( \frac{f}{f_{z2}} \right)^2} \right]
\]

\[
\frac{1}{\sqrt{1 + \left( \frac{f}{f_{p1}} \right)^2} \sqrt{1 - \left( \frac{f}{f_n} \right)^2} + \left( \frac{f}{f_n Q_p} \right)^2}.
\]

\[
\arg H(f) = \tan^{-1} \left( \frac{f}{f_{z1}} \right) - \tan^{-1} \left( \frac{f}{f_{z2}} \right) - \tan^{-1} \left( \frac{f}{f_{p1}} \right) - \tan^{-1} \left( \frac{f}{f_n Q_p} \right) - \frac{1}{1 - \left( \frac{f}{f_n} \right)^2}.
\]

- Plot them with Mathcad® for instance.

RHPZ
Fixed-Frequency Current-Mode

- Extract the information at the selected crossover frequency

\[
|H(s)| \quad \angle H(s) \quad \text{dB} \\
\text{Hz}
\]

\[
|H(3 \text{kHz})| = -16.3 \text{ dB} \quad \arg H(3 \text{ kHz}) = -23^\circ
\]
Fixed-Frequency Current-Mode

- The compensation strategy is the following:
  - compensate the gain loss at $f_c$ so that: $|G(3\text{kHz})| = +16.3\text{dB}$
  - evaluate the boost in phase at $f_c$ to get phase $70^\circ$ margin:
    \[
    \text{Boost} = \text{PM} - \arg H(f_c) - 90 = 3.15^\circ
    \]
      
      Boost = 0 select type 1 – origin pole
      Boost < 90° select type 2 – origin pole, 1 pole, 1 zero

- $k$-factor can be used to place the pole and the zero
  \[
  k = \tan \left( \frac{\text{boost}}{2} + 45 \right) \approx 1 \quad \rightarrow \quad \text{poles and zeros are coincident}
  \]
  \[
  f_{pk1} = kf_c = 1 \times 3k = 3\text{kHz} \quad f_{zk1} = \frac{f_c}{k} = \frac{3k}{1} = 3\text{kHz}
  \]
Fixed-Frequency Current-Mode

- Plot the compensator transfer function

\[
|G(s)| = 20 \log_{10} \left[ G \frac{f}{f_{pk}} \sqrt{1+\left(\frac{f}{f_{zk1}}\right)^2} \right]
\]

\[
\angle G(s) = \tan^{-1} \left( \frac{f}{f_{zk1}} \right) - \tan^{-1} \left( \frac{f}{f_{pk1}} \right) \frac{180}{\pi}
\]

\[
\\\text{boost} = \left[ \frac{\tan^{-1} \left( \frac{f}{f_{zk1}} \right) - \tan^{-1} \left( \frac{f}{f_{pk1}} \right) \frac{180}{\pi}}{\frac{f}{f_{pk0}}} \right]^{1/2}
\]
Fixed-Frequency Current-Mode

- Plot the loop gain transfer function and check the margins

- Sweep ESR, $C_{out}$, $R_{load}$ and verify the results
In case the converter transitions to DCM, update the equation!

Yes, analytical analysis is long and tedious.
But, it teaches where the threats are and how to deal with!
Variable-Frequency Current-Mode

- Observing the waveforms helps us to derive an average model

\[ I_a(t) \]

\[ I_c(t) \]

\[ I_{peak} \]

\[ dT_{sw} \]

\[ T_{sw} \]

- It gives birth to a large-signal model

\[ a \]

\[ la \]

\[ d1.lc \]

\[ lc \]

\[ c \]

\[ Vc/(2*Ri) \]

\[ V_{in} \]

\[ V_{out} \]

\[ V_{iout} \]

\[ V_{L} \]

\[ d1 \]

\[ Sense \] resistor

\[ \langle I_c(t) \rangle_{T_{sw}} = \frac{I_{peak}}{2} \]

\[ V_c = \frac{2RP_{out}(V_{out} + NV_{in})}{V_{in}V_{out}} \]

\[ T_{sw} = \frac{V_cL_p}{R_i}\left(\frac{1}{V_{in}} + \frac{N}{V_{out}}\right) \]

\[ d_1 = \frac{2P_{out}R_i}{V_cV_{in}} \]
Variable-Frequency Current-Mode

- Linearization is needed to get a small-signal model
- Implement this small-signal model in a flyback configuration

http://cbasso.pagesperso-orange.fr/Spice.htm
Variable-Frequency Current-Mode

- Derive the transfer function and isolate poles and zeros

\[
\frac{\hat{v}_{\text{out}}(s)}{\hat{v}_c(s)} = G_0 \left( \frac{1 + \frac{s}{s_{z1}}}{1 + \frac{s}{s_{p1}}} \right) \left( \frac{1 - \frac{s}{s_{z2}}}{2NR_i \left( \frac{2V_{\text{out}}}{NV_{\text{in}}} + 1 \right)} \right)
\]

- Then plot the function

\[
G_0 = \frac{R_{\text{load}} \text{Div}}{2 NR_i \left( \frac{2V_{\text{out}}}{NV_{\text{in}}} + 1 \right)}
\]

\[
f_{p1} = \frac{1}{2\pi R_{\text{load}} C_{\text{out}}} \frac{2M + 1}{M + 1}
\]

\[
f_{z1} = \frac{1}{2\pi R_{\text{ESR}} C_{\text{out}}}
\]

\[
f_{z2} = \frac{R_{\text{load}}}{2\pi N^2 L_p} \frac{1}{M(1 + M)}
\]

Tailor \( G(s) \) to get the desired \( f_c \)
Use a SPICE Model to Stabilize the Converter

Automate the compensation!
Unveil the Transfer Function in a Second

\[ H(s) \]

- Power stage gain

\[ T(s) \]

- Loop gain

\[ \angle H(s) \]

\[ \angle T(s) \]

- \( f_c \)

- \( \phi_m \)
Course Agenda

- The Flyback Converter
- The Parasitic Elements
- How These Parasitics Affect your Design?
- Current-Mode is the Most Popular Scheme
- Fixed or Variable Frequency?
- More Power than Needed
- The Frequency Response
- Compensating With the TL431
How is regulation performed?

- Text books only describe op amps in compensators...

- The market reality is different: the TL431 rules!

I’m the law!

TL431  optocoupler
The TL431 Programmable Zener

- The TL431 is the most popular choice in nowadays designs
- It associates an open-collector op amp and a reference voltage
- The internal circuitry is self-supplied from the cathode current
- When the R node exceeds 2.5 V, it sinks current from its cathode

- The TL431 is a shunt regulator
A Rabbit and a (French) Snail…

- The TL431 lends itself very well to optocoupler control

- $R_{LED}$ must leave enough headroom over the TL431: upper limit!
Understanding the Fast Lane Drawback

- This LED resistor is a design limiting factor in low output voltages:

\[
R_{LED,\text{max}} \leq \frac{V_{out} - V_f - V_{TL431,\text{min}}}{V_{dd} - V_{CE,\text{sat}} + I_{\text{bias}} \cdot CTR_{\text{min}} \cdot R_{\text{pullup}}} \cdot R_{\text{pullup}} \cdot CTR_{\text{min}}
\]

- When the capacitor \( C_1 \) is a short-circuit, \( R_{LED} \) fixes the fast lane gain:

\[
V_{FB}(s) = -CTR \cdot R_{\text{pullup}} \cdot I_1
\]

\[
I_1 = \frac{V_{out}(s)}{R_{LED}}
\]

\[
\frac{V_{FB}(s)}{V_{out}(s)} = -CTR \cdot \frac{R_{\text{pullup}}}{R_{LED}}
\]

This resistor plays a role in dc too!
The Static Gain Limit

- Let us assume the following design:

\[ V_{out} = 5 \, V \]
\[ V_f = 1 \, V \]
\[ V_{TL431,min} = 2.5 \, V \]
\[ V_{dd} = 4.8 \, V \]
\[ V_{CE,sat} = 300 \, mV \]
\[ I_{bias} = 1 \, mA \]
\[ CTR_{min} = 0.3 \]
\[ R_{pullup} = 20 \, k\Omega \]

\[ R_{LED,max} \leq \frac{5 - 1 - 2.5}{4.8 - 0.3 + 1m \times 0.3 	imes 20k} \times 20k \times 0.3 \]

\[ R_{LED,max} \leq 857 \, \Omega \]

- In designs where \( R_{LED} \) fixes the gain, \( G_0 \) cannot be below 17 dB

\[ G_0 > CTR \frac{R_{pullup}}{R_{LED}} > 0.3 \frac{20}{0.857} > 7 \text{ or } \approx 17 \, dB \]

\[ \rightarrow \text{ You cannot “amplify” by less than 17 dB} \]
Forbidden Compensation Areas

- You must identify the areas where compensation is possible

![Diagram showing dB vs. frequency with regions marked as 'Not ok' and 'ok'.]

- Requires less than 17 dB of gain
- Requires 17 dB or more

\[ f_c > 500 \text{ Hz} \]
Injecting Bias Current

- Make sure enough current always biases the TL431.
- If not, its open-loop suffers – a 10-dB difference can be observed!

\[ I_{bias} = 1.3 \, mA \]
\[ I_{bias} = 300 \, \mu A \]

\[ R_{bias} = \frac{1}{1m} = 1 \, k\Omega \]
Small-Signal Analysis

- The TL431 is an open-collector op amp with a reference voltage.
- Neglecting the LED dynamic resistance, we have:

\[
V_{out}(s) = V_{out}(s) - V_{op}(s)
\]

\[
I_1(s) = \frac{V_{out}(s) - V_{op}(s)}{R_{LED}}
\]

\[
V_{op}(s) = -V_{out}(s) \frac{sC_1}{R_{upper}} = -V_{out}(s) \frac{1}{sR_{upper}C_1}
\]

\[
I_1(s) = V_{out}(s) \frac{1}{R_{LED}}[1 + \frac{1}{sR_{upper}C_1}]
\]

We know that:

\[
V_{FB}(s) = -CTR \cdot R_{pullup} \cdot I_1
\]

\[
\frac{V_{FB}(s)}{V_{out}(s)} = -\frac{R_{pullup}CTR}{R_{LED}} \left[1 + \frac{sR_{upper}C_1}{sR_{upper}C_1}\right]
\]
Creating a High-Frequency Pole

- In the previous equation we have:
  - a static gain \( G_0 = \text{CTR} \frac{R_{\text{pullup}}}{R_{\text{LED}}} \)
  - a 0-dB origin pole frequency \( \omega_{po} = \frac{1}{C_1 R_{\text{upper}}} \)
  - a zero \( \omega_z = \frac{1}{R_{\text{upper}} C_1} \)

- We are missing a pole for the type 2!

\[
\frac{V_{FB}(s)}{V_{out}(s)} = -\frac{R_{\text{pullup}} \text{CTR}}{R_{\text{LED}}} \left[ \frac{1 + sR_{\text{upper}} C_1}{sR_{\text{upper}} C_1 \left(1 + sR_{\text{pullup}} C_2\right)} \right]
\]

Add a cap. from collector to ground
Understanding the Optocoupler Pole

- The optocoupler also features a parasitic capacitor
  - it comes in parallel with $C_2$ and must be accounted for

\[ C_2 = C \parallel C_{\text{opto}} \]

\[ V_{\text{dd}} \]

\[ V_{FB}(s) \]

\[ R_{\text{pullup}} \]

\[ C \]

\[ V_{\text{out}}(s) \]
Extracting the Pole

- The optocoupler must be characterized to know where its pole is.

- Adjust $V_{bias}$ to have $V_{FB}$ at 2-3 V to be in linear region, then ac sweep.

- The pole in this example is found at 4 kHz.

\[ C_{opto} = \frac{1}{2\pi R_{pullup} f_{pole}} = \frac{1}{6.28 \times 20k \times 4k} \approx 2 \text{ nF} \]

Another design constraint!
The TL431 in a Type 1 Compensator

- To make a type 1 (origin pole only) neutralize the zero and the pole

\[
\begin{align*}
V_{FB}(s) &= -\frac{R_{pullup}}{R_{LED}} CTR \left[ \frac{1 + sR_{upper}C_1}{sR_{upper}C_1 \left(1 + sR_{pullup}C_2\right)} \right] \\
V_{out}(s) &= \frac{1}{s - \frac{R_{pullup}}{R_{LED}C_2}} \left( \frac{1}{sR_{upper}C_1} \right)
\end{align*}
\]

\[
\begin{align*}
sR_{upper}C_1 &= sR_{pullup}C_2 \\
C_1 &= \frac{R_{pullup}}{R_{upper}}C_2 \\
\omega_{po} &= \frac{1}{R_{upper}R_{LED}C_1}
\end{align*}
\]

- Once neutralized, you are left with an integrator

\[
G(s) = \frac{1}{\omega_{po}} \quad \implies \quad |G(f_c)| = \frac{f_{po}}{f_c} \quad \implies \quad f_{po} = G_{f_c}f_c \\
C_2 = \frac{CTR}{2\pi f_{po}R_{LED}}
\]
A Type 1 Design Example

- We want a 5-dB gain at 5 kHz to stabilize the 5-V converter

\[
\begin{align*}
V_{out} &= 5 \text{ V} \\
V_f &= 1 \text{ V} \\
V_{TL431,\text{min}} &= 2.5 \text{ V} \\
V_{dd} &= 4.8 \text{ V} \\
V_{CE,\text{sat}} &= 300 \text{ mV} \\
I_{\text{bias}} &= 1 \text{ mA} \\
\text{CTR}_{\text{min}} &= 0.3 \\
R_{\text{pullup}} &= 20 \text{ k}\Omega \\
G_{f_c} &= 10^{\frac{5}{20}} = 1.77 \\
f_c &= 5 \text{ kHz}
\end{align*}
\]

Apply 15% margin

\[
R_{\text{LED,\text{max}}} \leq 857 \Omega \quad \Rightarrow \quad R_{\text{LED}} = 728 \Omega
\]

\[
C_2 = \frac{\text{CTR}}{2\pi G_{f_c} f_c R_{\text{LED}}} = \frac{0.3}{6.28 \times 1.77 \times 5 \times 728} \approx 7.4 \text{ nF}
\]

\[
C_{\text{opto}} = 2 \text{ nF}
\]

\[
C = 7.4n - 2n = 5.4 \text{ nF} \\
C_1 = \frac{R_{\text{pullup}}}{R_{\text{upper}}} C_2 \approx 14.7 \text{ nF}
\]
Simulation of the Type 1

- SPICE can simulate the design – automate elements calculations…

Parameters:
- $V_{out}=5$
- $V_f=1$
- $V_{ref}=2.5$
- $V_{dd}=4.8$
- $I_{bias}=1m$

$$A = V_{out} - V_f - V_{ref}$$
$$B = V_{dd} - V_{CEsat} + I_{bias} \cdot CTR \cdot R_{pullup}$$
$$R_{upper} = (V_{out} - 2.5) / 250u$$
$$f_c = 5k$$
$$G_f = 5$$

$$G = 10^*(-G_f/20)$$
$$\pi = 3.14159$$

$$F_{po} = G \cdot f_c$$
$$R_{pullup} = 20k$$
$$R_{LED} = R_{max} \cdot 0.85$$

$$C_{1} = C_{pole1} \cdot R_{pullup} / R_{upper}$$

$$R_{max} = (A / B) \cdot R_{pullup} \cdot CTR$$

$$R_{upper} = (V_{out} - 2.5) / 250u$$
$$f_c = 5k$$

$$G_f = -5$$
$$G = 10^{e(G_f/20)}$$

$$F_{po} = G \cdot f_c$$

Automatic bias point selection
Type 1 Simulation Results

- The pullup resistor is 1 kΩ and the target now reaches 5 dB
The TL431 in a Type 2 Compensator

- Our first equation was already a type 2 definition, we are all set!

- Just make sure the optocoupler contribution is involved…

\[ G_0 = \text{CTR} \frac{R_{\text{pullup}}}{R_{\text{LED}}} \]

\[ \omega_{z_1} = \frac{1}{R_1C_1} \]

\[ \omega_{p_1} = \frac{1}{R_{\text{pullup}}C_2} \]
Deriving Component Values for the Type 2

- You need to provide a 15-dB gain at 5 kHz with a 50° boost.
  
  \[ f_p = \left[ \tan(\text{boost}) + \sqrt{\tan^2(\text{boost}) + 1} \right] f_c = 2.74 \times 5k = 13.7 \text{ kHz} \]
  
  \[ f_z = f_c^2 / f_p = 25k / 13.7k \approx 1.8 \text{ kHz} \quad G_0 = \text{CTR} \frac{R_{\text{pullup}}}{R_{\text{LED}}} = 10^{15/20} = 5.62 \]

- With a 250-µA bridge current, the divider resistor is made of:
  
  \[ R_{\text{lower}} = 2.5 / 250u = 10 \text{ kΩ} \quad R_1 = (12 - 2.5) / 250u = 38 \text{ kΩ} \]

- The pole and zero respectively depend on \( R_{\text{pullup}} \) and \( R_1 \):
  
  \[ C_2 = 1/2\pi f_p R_{\text{pullup}} = 581 \text{ pF} \quad C_1 = 1/2\pi f_z R_1 = 2.3 \text{ nF} \]

- The LED resistor depends on the needed mid-band gain:
  
  \[ R_{\text{LED}} = \frac{R_{\text{pullup}} \text{CTR}}{G_0} = 1.06 \text{ kΩ} \quad \text{ok} \quad R_{\text{LED,max}} \leq 4.85 \text{ kΩ} \]
Checking the Optocoupler Contribution

- The optocoupler is still at a 4-kHz frequency:
  \[ C_{pole} \approx 2 \text{nF} \] Already above!

- Type 2 pole capacitor calculation requires a 581-pF cap.!

  The bandwidth cannot be reached, reduce \( f_c \)!

- For noise purposes, we want a minimum of 100 pF for \( C \)

- With a total capacitance of 2.1 nF, the highest pole can be:
  \[
  f_{pole} = \frac{1}{2\pi R_{pullup} C} = \frac{1}{6.28 \times 20k \times 2.1n} = 3.8 \text{ kHz}
  \]

- For a 50° phase boost and a 3.8-kHz pole, the crossover must be:
  \[
  f_c = \frac{f_p}{\tan(\text{boost}) + \sqrt{\tan^2(\text{boost}) + 1}} \approx 1.4 \text{ kHz}
  \]
Placing the Zero in the Transfer Function

- The zero is then simply obtained:
  \[ f_z = \frac{f_c^2}{f_p} = 516 \text{ Hz} \]
- We can re-derive the component values and check they are ok
  \[ C_2 = \frac{1}{2\pi f_p R_{\text{pullup}}} = 2.1 \text{ nF} \quad C_1 = \frac{1}{2\pi f_z R_1} = 8.1 \text{ nF} \]
- Given the 2-nF optocoupler capacitor, we just add 100 pF
- In this example, \( R_{\text{LED, max}} \) is 4.85 k\( \Omega \)
  \[ G_0 > CTR \frac{R_{\text{pullup}}}{R_{\text{LED}}} > 0.3 \frac{20}{4.85} > 1.2 \text{ or } \approx 1.8 \text{ dB} \]
- You cannot use this type 2 if an attenuation is required at \( f_c \)!
The 1-dB gain difference is linked to $R_d$ and the bias current.

- $|G(s)|$ graph shows 14 dB @ 1.4 kHz.
- $\arg G(s)$ graph shows 50°.
Design Example 1 – a Single-Stage PFC

- The single-stage PFC is often used in LED applications
- It combines isolation, current-regulation and power factor correction
- Here, a constant on-time BCM controller, the **NCP1608**, is used
Design Example 1 – a Single-Stage PFC

- Once the converter elements are known, ac-sweep the circuit
- Select a crossover low enough to reject the ripple, e.g. 20 Hz

![Graph showing dB and phase angle vs frequency]

- $|H(s)|$ vs frequency
- $\arg H(s)$ vs frequency
Design Example 1 – a Single-Stage PFC

- Given the low phase lag, a type 1 can be chosen
- Use the type 2 with fast lane removal where $f_p$ and $f_z$ are coincident

\[ G(s) = \frac{6.1 \, k\Omega}{15 \, V} \]

\[ 10 \, k\Omega \]

\[ 586 \, nF \]

\[ 13.6 \, k\Omega \]

\[ 395 \, nF \]

\[ 5 \, V \]

\[ 20 \, k\Omega \]

\[ t_{on} \] generation

\[ f_c = 19 \, Hz \]

\[ \varphi_m = 90^\circ \]

\[ \arg T(s) \]

\[ |T(s)| \]
Design Example 1 – a Single-Stage PFC

- A transient simulation helps to test the system stability

- $I_{LED}(t)$
- $V_{FB}(t)$
- $I_{in}(t)$

- $V_{in} = 100$ V rms
Design Example 2: a DCM Flyback Converter

- We want to stabilize a 20-W DCM adapter
- $V_{in} = 85$ to 265 V rms, $V_{out} = 12$ V/1.7 A
- $F_{sw} = 65$ kHz, $R_{pullup} = 20$ kΩ
- Optocoupler is SFH-615A, pole is at 6 kHz
- Cross over target is 1 kHz
- Selected controller: NCP1216

1. Obtain a power stage open-loop Bode plot, $H(s)$
2. Look for gain and phase values at cross over
3. Compensate gain and build phase at cross over, $G(s)$
4. Run a loop gain analysis to check for margins, $T(s)$
5. Test transient responses in various conditions
Design Example 2: a DCM Flyback Converter

- Capture a SPICE schematic with an averaged model

- Look for the bias points values: $V_{out} = 12\,\text{V}$, ok
Design Example 2: a DCM Flyback Converter

- Observe the open-loop Bode plot and select $f_c$: 1 kHz

**Magnitude at 1 kHz:** -23 dB

**Phase at 1 kHz:** -70°
Design example 2: a DCM flyback converter

- Apply $k$ factor or other method, get $f_z$ and $f_p$
- $f_z = 3.5 \text{ kHz}$, $f_p = 4.5 \text{ kHz}$

\[ C = 3.8 \text{nF} \]
\[ C_2 = 3.8n - 1.3n \approx 2.5 \text{nF} \]

\[ C_{\text{opto}} = 1.3 \text{nF} \]
Design example 2: a DCM Flyback Converter

Check loop gain and watch phase margin at $f_c$

Crossover
1 kHz

$\varphi_m = 60^\circ$

$T(s)\bigg|_{\text{Crossover}}$

arg $T(s)$
Design Example 2: a DCM Flyback Converter

- Sweep ESR values and check margins again

\[
V_{\text{out}}(t)
\]

- High line
- Low line

100 mV

200 mA to 2 A in 1 A/µs
Conclusion

- The flyback converter hides several parasitic elements
- Understanding where they hide and how they move is key!
- Despite CM overwhelming presence, QR designs grow
- CM is a 3rd-order system whereas QR is 1st order
- TL431 lends itself well for compensation, watch the optocoupler!
- SPICE eases and speed-up the design
- Always check theoretical assumptions with bench measurement

Merci !
Thank you!
Xiè-xie!