The TL431 in Switch-Mode Power Supplies loops: part I

Christophe Basso, Petr Kadanka – ON Semiconductor
14, rue Paul Mesplé – BP53512 - 31035 TOULOUSE Cedex 1 - France

The technicall literature on loop control abounds with design examples of compensators implementing an operational amplifier (op amp). If the op amp certainly represents a possible way to generate an error signal, the industry choice for this function has been different for many years: almost all consumer power supplies involve a TL431 placed on the isolated secondary side to feed the error back to the primary side via an opto coupler. Despite its similarities with its op amp cousin, the design of a compensator around a TL431 requires a good understanding of the device operation. This first part explores the internal structure of the device and details how its biasing conditions can degrade the performance of the loop.

A band-gap-based component

Figure 1 shows the internal schematic of a TL431 made in a bipolar technology. Before we detail the usage of the component itself in a power supply loop, we believe it is important to understand how the device operates. The bias points are coming from a simple simulation setup where the device was used as a reference voltage. This configuration implies a connection between it reference point, *ref*, and the cathode *k*, while the anode *a* is grounded, making the device behave as an active 2.5-V zener diode.

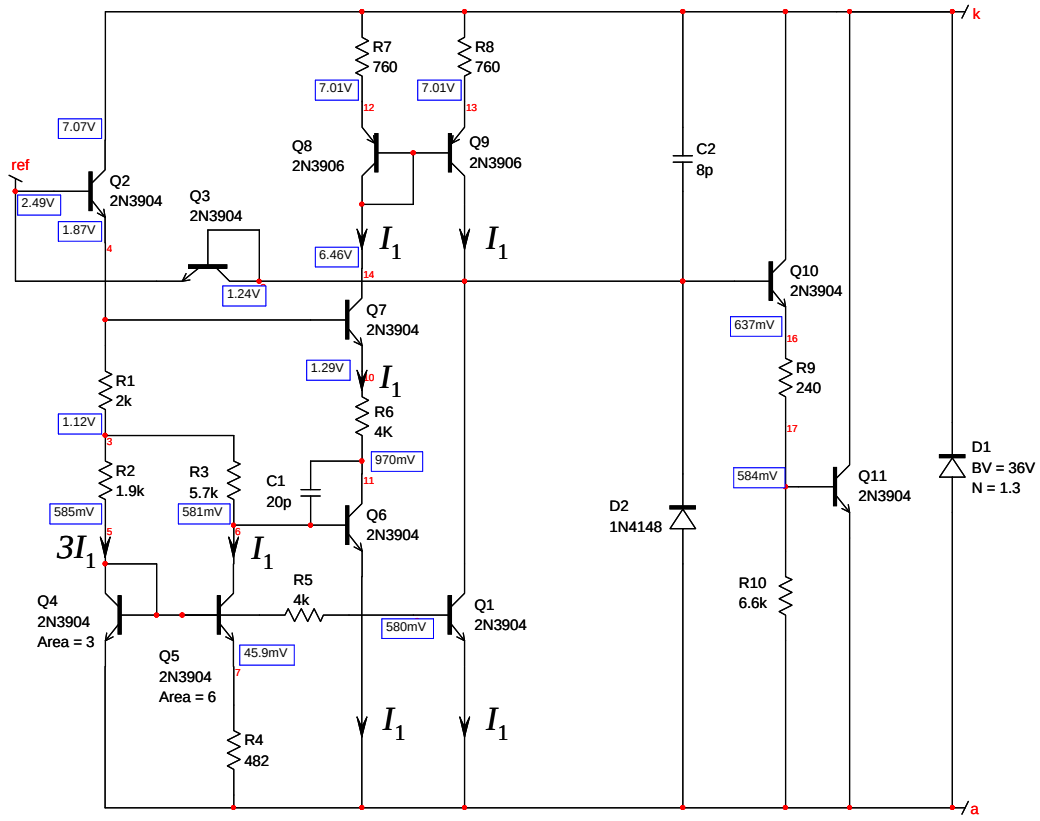

Figure 1 : the internal schematic of a typical TL431 from ON Semiconductor where bias points in voltage and current have been captured at the equilibrium.

In classical loop-control configuration, the TL431 observes a fraction of the output voltage seen by its *ref* pin and converts it into an output current sank between the cathode and the anode. As such, the device can be considered as a transconductance amplifier. The TL431 internal reference circuit works around a popular structure called a *band-gap*. The description of a band-gap is outside the scope of this article but basically, the principle consists in balancing the negative temperature coefficient of a junction (a transistor V_{BE}) by a thermal voltage, V_T, affected by a positive temperature coefficient. When summed together, these voltages nicely compensate to form a temperature-compensated reference voltage.

To simplify the analysis, we will assume that the current gain β of all transistors used in the TL431 is very high, implying negligible base currents. The secret of operating the TL431 lies in the subtle equilibrium imposed by Q_9 and Q_1: when conditions are met, e.g. V_{out} reached its target and V_{ref} equals 2.5 V, both Q_9 and Q_1

share the same current I_1: V_{ka} remains constant. Any modification in this condition, for instance brought by a set point variation or an increased output power demand on the regulated converter, will either force either Q_9 to source more current or Q_1 to increase its sinked current, changing the bias of the output darlington configuration made around Q_{10} and Q_{11}. This action respectively brings V_{ka} down or up and forces a current variation in the LED diode attached to the TL431 cathode in a power supply loop application.

At the equilibrium, if we neglect the base currents, the current mirror brought by Q_8 and Q_9 duplicates I_1 which also circulates in Q_7 and Q_6. Because of the current mirror arrangement between Q_1 and Q_4, the same current but scaled up by a ratio of 1 to 3 flows in Q_4 as well. This is confirmed by identical voltage drops across R_2 and R_3 (≈530 mV), also featuring a 1 to 3 ratio (1.9 kΩ and 5.7 kΩ):

$$I_{C,Q_5} = \frac{I_{C,Q_4}}{3} = I_{C,Q_1} = I_1 \tag{1}$$

Q_7 is wired in a cascode configuration and helps to shield Q_6 voltage bias against the variations on the *k* terminal that would otherwise be duplicated minus a V_{BE} on Q_6 collector.

In Figure 1, the band-gap is made by associating transistors Q_4 and Q_5 together with the emitter resistor R_4. The *area* parameter on both devices indicates that Q_4 is "equivalent" to three transistors in parallel whereas Q_5 is made of six paralleled transistors. Otherwise stated, the emitter size of the transistor Q_5 is twice that of transistor Q_4 given respective *area* parameters of 6 and 3. Therefore, not only the current densities *J* in their emitters are linked ($J_4 = 6J_5$), but their saturation currents I_S is also affected by this relationship:

$$I_{S,Q_5} = 2I_{S,Q_4} \tag{2}$$

The reference voltage

Now, it is interesting to calculate how the 2.5-V reference is actually established in the TL431. To do so, we need to start with current values flowing through Q_4 and Q_5. Capitalizing on the equilibrium, we know that I_1 circulates in Q_1 and $3I_1$ in Q_4 (1) but thanks to the ratio of resistor R_2 and R_3, I_1 also naturally flows in Q_5. We can write the following equation for voltage difference between base terminals of Q_4,Q_5 and the anode terminal:

$$V_{BE4} = V_{BE5} + I_1 R_4 \tag{3}$$

The base-emitter voltage of a bipolar transistor can be calculated from its collector current I_C according following equation:

$$V_{BE} = V_T \ln\left(\frac{I_C}{I_S}\right) \tag{4}$$

Where $V_T = \frac{kT}{q} \approx 25\,mV$ at a 27-°C room temperature or 300 Kelvin. In this equation, I_S is the transistor saturation current (directly proportional to its emitter size), *k* is the Boltzmann constant (1.38×10^{-23}) and *q* is the electron charge equal to $1.601\times10^{-19}\ C$.

We know from (2) that the saturation current of Q_5 is twice the saturation current of Q_4. We can therefore update and substitute (4) in (3):

$$V_T \ln\left(\frac{3I_1}{I_S}\right) = V_T \ln\left(\frac{I_1}{2I_S}\right) + R_4 I_1 \tag{5}$$

Re-arranging and factoring V_T gives:

$$V_T\left[\ln\left(\frac{3I_1}{I_S}\right) - \ln\left(\frac{I_1}{2I_S}\right)\right] = R_4 I_1 \tag{6}$$

We know that $\ln a - \ln b = \ln\left(\frac{a}{b}\right)$, therefore:

$$V_T \ln\left(\frac{3I_1}{I_S}\frac{2I_S}{I_1}\right) = V_T \ln 6 = R_4 I_1 \tag{7}$$

From which we can extract the value of the current I_1:

$$I_1 = \frac{V_T \ln 6}{R_4} \tag{8}$$

Based on the value of R_4 which is 482 Ω, we can calculate the value of I_1:

$$I_1 = \frac{26m \times 1.79}{482} \approx 97\ \mu A \tag{9}$$

Knowing this current, the drop over the collector loads R_2 and R_3 can quickly be derived by ohm's law:

$$V_{R_2} = V_{R_3} = 3R_2 I_1 = R_3 I_1 = 1.9k \times 97u = 5.7k \times 97u = 553\ mV \tag{10}$$

which is not far away from the bias point calculated by SPICE. As R_1 is crossed by the sum of the currents flowing into Q_4 ($3I_1$) and Q_5 (I_1), its voltage drop is simply:

$$V_{R_1} = 4R_1 I_1 = 2k \times 4 \times 97u = 776\ mV \tag{11}$$

Finally, if we stack up all the voltages we have calculated and assume transistors V_{BE} of 580 mV, we obtain the reference level we look for:

$$V_{ref} = V_{R_1} + V_{R_2} + V_{BE2} + V_{BE4} = 0.553 + 0.776 + 0.58 + 0.58 = 2.49\ V \tag{12}$$

This is the value displayed in Figure 1 over the *ref* node.

The frequency compensation of the TL431 is performed by the capacitors C_1, C_2 and the resistor R_6.

The need for bias current

We explained that the condition for equilibrium is reached when V_{ref} equals 2.49 V. Now, if the voltage applied on V_{ref} changes, for instance increases, the voltage change is propagated on the emitter of Q_2 and forces a current change in R_1. This change will now be seen on Q_4 and Q_5 currents, respectively conveying the information to Q_1 and Q_6. To that respect, you could see Q_1 and Q_6 working as a differential amplifier. However, as more current flows in Q_4, its path will naturally offer a larger gain to activate Q_1, sinking more current to ground that Q_6 does: V_{ka} is pulled down.

We could analytically calculate the transconductance gain of the TL431 but we can also deduce it from the characterization curve shown in Figure 2. From this curve, we can read a dc gain of 55 dB. This value, together with the 230-Ω pull-up resistor implies a *gm* value of:

$$gm = \frac{10^{\frac{55}{20}}}{230} = 2.44\ A/V \tag{13}$$

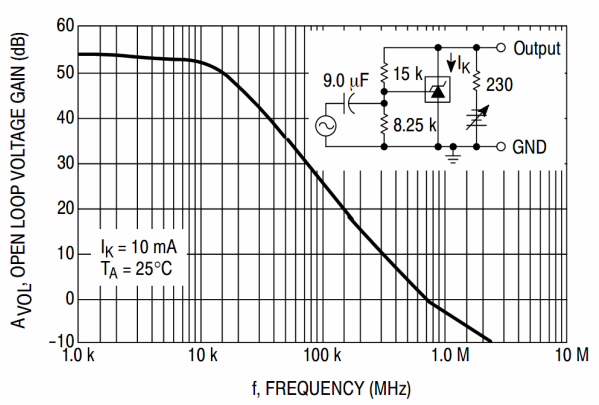

Figure 2 : the ac test is carried upon a TL431 loaded by a 230-Ω resistor. The injected current is around 10 mA.

As the caption details, the cathode current was set to 10 mA during the measurement. A traditional zener diode needs some substantial bias current to make it operate far away from its knee. Otherwise, the dynamic impedance exhibited by the diode is affected and the zener voltage depends on the injected current. Despite being a kind of active zener diode, the TL431 makes no exception to that particular rule. You need to inject current in its cathode to get the best from the device. We have run simulations on the transistor-level TL431 model to check where the knee sharpens. This is what appears in Figure 3.

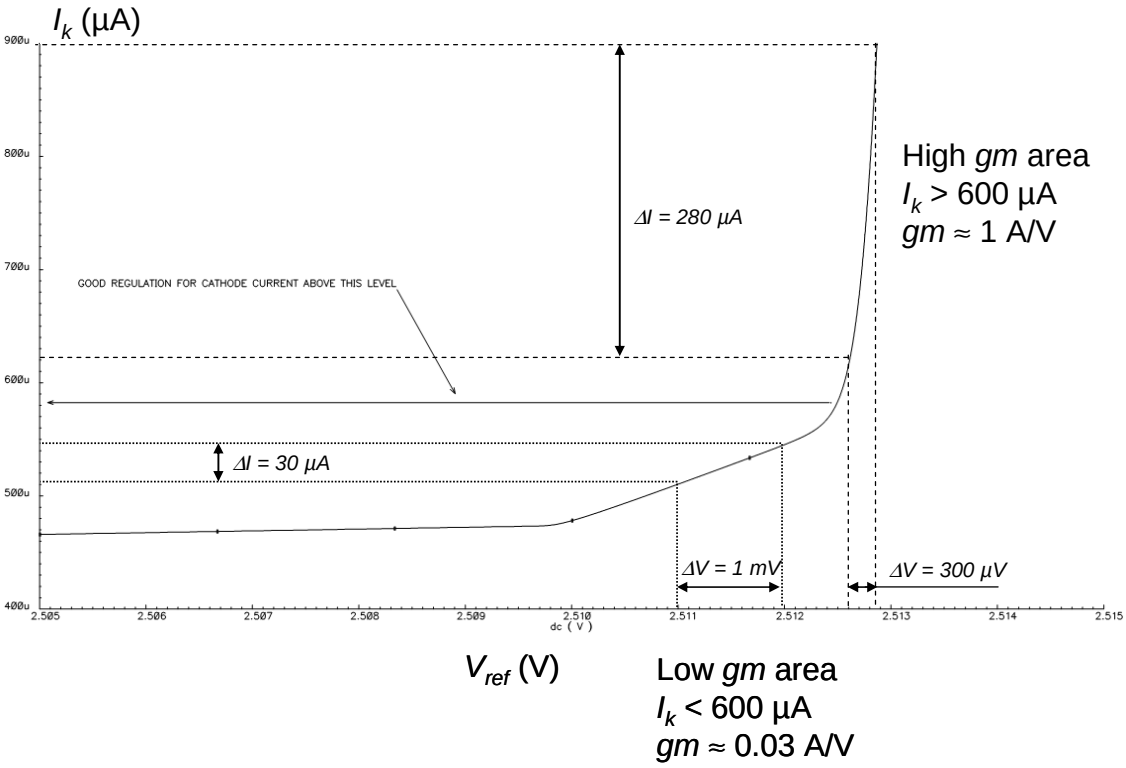

Figure 3 : from this figure, we can clearly see the appearance of the knee below a 600-µA injected current. Below this value, the transconductance gain *gm* is rather poor.

In this drawing, we can identify a region below which the *gm* of the device is low, with values in the vicinity of 30 mA/V. As the cathode current increases, the transconductance improves and reaches up to 1 A/V. As more current is injected, values up to what is given by (13) are obtained.

One way to inject more current is described in Figure 4 where a simple resistor connected in parallel with the opto coupler LED increases the current injected in the TL431. As the LED forward drop is around 1 V, a paralleled 1-kΩ resistor forms a simple 1-mA generator which sums up with the feedback current flowing through the LED. Please note that decreasing the LED series resistor R_{LED} does not change the TL431 current as this current is imposed by the primary-side feedback current I_C, reflected in the LED by the opto coupler current

transfer ratio (CTR). Changing R_{LED} value affects the mid-band gain but not the TL431 bias as the system operates in a closed-loop form. Reference [1] includes all calculation details related to the TL431 bias calculations.

Finally, what current shall we inject in the TL431? The specifications state a 1-mA minimum current and Ref. [2] claims a minimum of 5 mA to obtain decent performance. What value must thus be selected? Well, besides the open-loop gain that is affected by the bias current, the consumption on the output voltage also plays a role in the selection. When you chase every tens of mW to stay below a 100-mW input power, you understand that you cannot afford to lose precious power in a bias current that is useless in no-load conditions. High-volume notebook adapters deal with a 1-mA extra bias current on top of the natural feedback current seen in the LED. The total bias in the TL431 is thus in the vicinity of 1.5 mA and experience shows that it is often good enough to reach adequate performance without sacrificing the standby power.

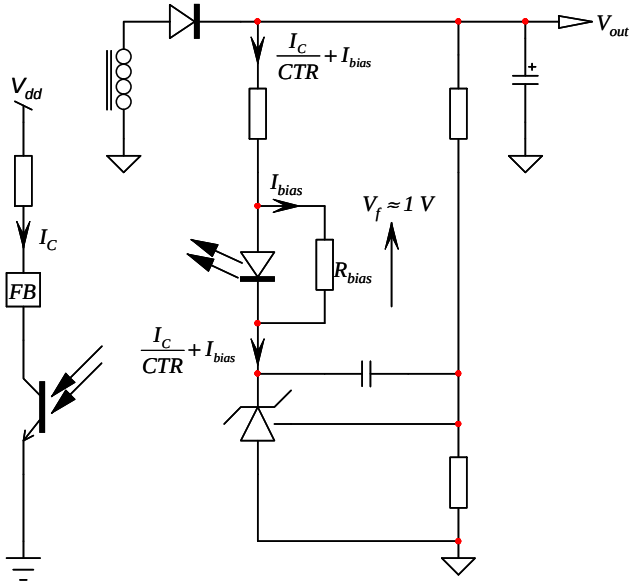

Figure 4 : a simple resistor in parallel with the opto coupler LED creates a free current source generator.

To demonstrate this fact, we have built a simple test fixture where a compensator was assembled as suggested by Figure 4. The collector current reflected through its CTR in the LED established to around 300 µA. We captured a plot without added bias current, letting these 300 µA only flow in the TL431. Then, a 1-kΩ resistor was put across the optocoupler LED to increase the bias current in the TL431 to roughly 1.3 mA. As one can immediately see in Figure 5, the open loop gain nicely benefited from this added bias current.

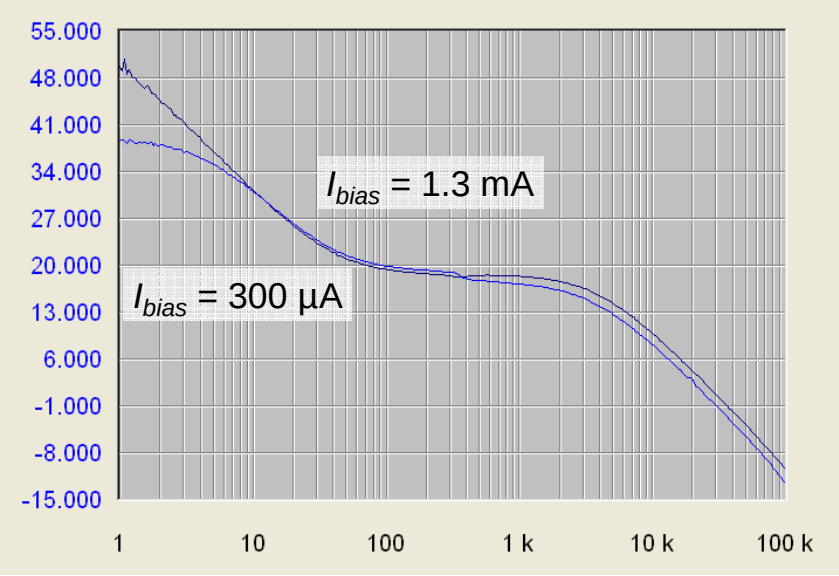

Figure 5 : the dc gain of the TL431 clearly benefits from an added bias current.

Conclusion

This article introduces the reader to the internal schematic of the TL431. Without entering into the real band-gap operation, it is important to understand how the part operates and the performance you can expect in relationship to its bias current. Readers further interested by the subject can visit Ref. [3] link where the author has gathered a lot of data on voltage reference designs. Now that we know how to bias the TL431, we will see in a next paper how to make a type-2 error amplifier out of it.

References

1. C. Basso, “Switch Mode Power Supplies: SPICE Simulations and Practical Designs”, McGraw-Hill, 2008
2. T. Tepsa, S. Suntio, “Adjustable Shunt Regulator Based Control Systems”, IEEE Power Electronics Letters, Vol. 1, N° 4, December 2003
3. http://www.circuitsage.com/bandgap.html

The TL431 in Switch-Mode Power Supplies loops: part II

Christophe Basso – ON Semiconductor
14, rue Paul Mesplé – BP53512 - 31035 TOULOUSE Cedex 1 - France

The previous article covered the internal operation of the popular TL431, explaining why a sufficiently high bias current was necessary to obtain the best out of the three-pin device. This paper will now focus on the TL431 practical implementation in a compensation circuit. If most of the theory books cover operational-amplifiers-based (op amp) compensation circuits, you rarely see descriptions of these circuits using a TL431. This article will detail how to wire a TL431 in a type-2 configuration, creating the compensation scheme for current-mode operated converters such as the flyback or the forward.

Creating phase boost with poles and zeros

The principle behind loop compensation consists in ensuring safe phase and gain margins in all working conditions when the converter operates closed loop. Phase margin implies that the total phase rotation of the loop gain *T(s)* is less than -360° at the cross over frequency f_c. Gain margin, on the opposite, qualifies the distance between the loop gain module and the 0-dB axis at a frequency where the total phase rotation is -360°. To ensure these design conditions are respected, we must insert a compensation circuit *G(s)* whose task is to shape the loop gain to cross over the 0-dB axis at the selected frequency and exhibits sufficient phase and gain margins at the considered frequencies. How do we select the crossover frequency? Some designer arbitrarily chose 1/5th of the switching frequency for instance. A better way is to analytically derive the 0-dB crossover point depending on the maximum undershoot stated in your specification sheet. Ref. [1] describes a possible method to get there. Let us assume for the sake of the example that this crossover frequency is 1 kHz.

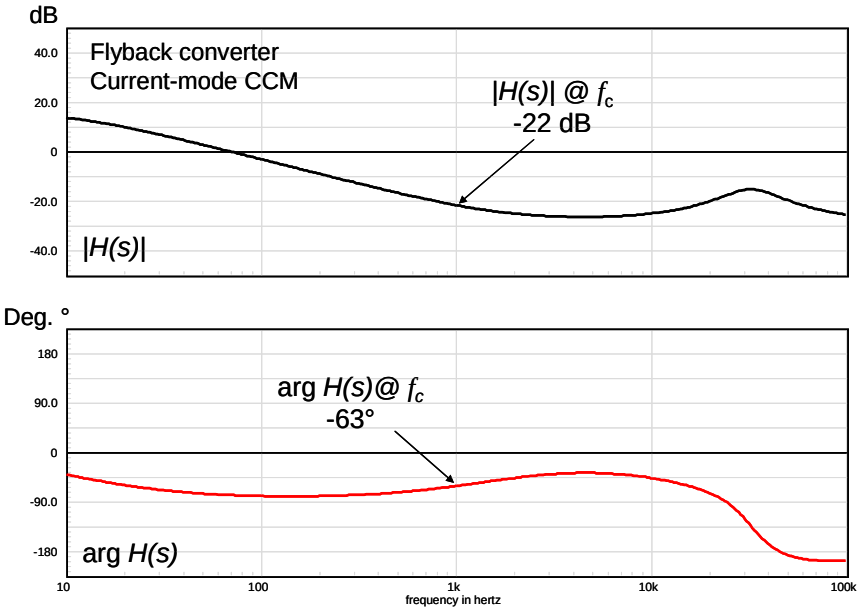

Figure 6 : the typical power conversion stage of a flyback converter operated in current mode.

The very first step starts from the power stage Bode plot. This is the function noted *H(s)* that appears in Figure 6. It is the response of an isolated current-mode CCM flyback converter featuring ramp compensation. This plot can either be obtained using bench test data, analytical analysis or by using a SPICE simulator [2]. From this graph, we can see a gain deficiency of -22 dB and a phase rotation of -63°, both values being read at the selected crossover frequency of 1 kHz. To obtain a good input rejection, a small output static error and a low output impedance, a large dc gain is needed. A pole at the origin will satisfy this requirement. Mathematically, a pole at the origin follows the form:

$$G(s) = \frac{1}{\frac{s}{\omega_p}} \tag{1}$$

Unfortunately, placing a pole right at the origin will induce a permanent phase rotation. Furthermore, because we use an op amp or a TL431 wired in an inverting configuration, the total phase rotation will amount to -270°:

$$\arg G(s) = \arg(1) - \arg\left(\frac{s}{\frac{s_{po}}{0}}\right) - \pi = -\arctan(\infty) - \pi = -\frac{\pi}{2} - \pi = -\frac{3\pi}{2} \tag{2}$$

Therefore, if we cumulate these -270° phase rotation with the -63° from the power stage, we end up with a total loop phase rotation of -333°. This gives us a 27-degree margin before hitting the -360° limit. This distance is the so-called *phase margin* and is noted φ_m. We know from loop control theory that the phase margin should be larger than 45° to obtain a fast non-ringing system. Actually, Ref. [3] suggests to design for 70°, offering the best trade-off between recovery speed and lack of overshoot. To expand the current 27-degree margin to 70°, we need to create a *phase boost*, occurring at the crossover frequency. This phase boost is exactly 43°:

$$BOOST = \varphi_m - \arg H(f_c) - 90° = 70° + 63 - 90 = 43° \tag{3}$$

A boost in phase can be created by combining poles and zeros together placed on the compensator transfer function *G(s)*. If we associate a zero and a pole together each occurring at different frequencies, the transfer function looks like the following equation:

$$G(s) = \frac{\left(1 + \frac{s}{s_{z1}}\right)}{\left(1 + \frac{s}{s_{p1}}\right)} \tag{4}$$

We know that a first-order zero, alone, rotates the phase from 0 to +90° whereas a first-order pole makes it turn from 0 to -90°. We say the zero *boosts* the phase whereas the pole *lags* it. Therefore, if we combine a zero and a pole, depending on the frequency at which we place them, we have a means to adjust the exact phase boost we are looking for. Evaluating the phase boost goes by calculating the argument of (4) in the frequency domain:

$$\arg G(f) = \arctan\left(\frac{f}{f_{z1}}\right) - \arctan\left(\frac{f}{f_{p1}}\right) \tag{5}$$

Where should we place the pole and zero in relationship to the crossover frequency? To have an idea, let us calculate the frequency at which (5) peaks, in other words, at what frequency the phase boost is maximum:

$$\frac{d\left(\arctan\left(\frac{f}{f_{z1}}\right) - \arctan\left(\frac{f}{f_{p1}}\right)\right)}{df} = 0 \tag{6}$$

Solving this equation leads to:

$$f = \sqrt{f_{z1} f_{p1}} \tag{7}$$

By placing the crossover frequency in the geometric mean of the pole and zero locations, we will benefit from the maximum phase boost we are looking for. Is this the only way to place the pole and zero? Clearly not. For instance, a pole can be placed to fight an annoying zero brought by the output capacitor Equivalent Series Resistance (ESR). The zero can be placed further down the frequency axis to help maintain stability in different operating conditions for instance. However, placing the pole and zero according to (7) is the simplest way to

start with. Now, back to our example, we need to boost the phase by 43° at a 1-kHz crossover frequency f_c. Where do we put the pole and the zero? By combining (5) and (7), we can solve for their respective position:

$$f_p = \left[\tan(boost) + \sqrt{\tan^2(boost)+1} \right] f_c = 2.3\,kHz \tag{8}$$

$$f_z = \frac{f_c^{\,2}}{f_p} \approx 435\,Hz \tag{9}$$

How do we make sure we cross over at 1 kHz then? By ensuring that the compensator for f = 1 kHz exactly exhibits a +22-dB gain. This gain is called the mid-band gain, often noted G_0.

To summarize, we need to create a compensation chain fulfilling the following specifications:

- 1 pole at the origin
- 1 zero
- 1 pole
- A mid-band gain G_0 at the crossover frequency

The type 2 with an op amp

In the literature, the aforementioned type of compensator is called a type 2 and is usually built around an op amp, as exemplified by Figure 7.

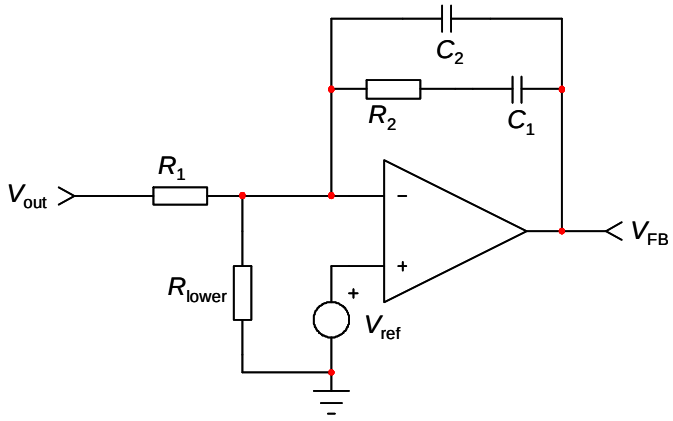

Figure 7: a type 2 compensator gathers an origin pole, a zero and a second pole.

The transfer function of such a configuration can be put under the following simplified form:

$$G(s) \approx -\frac{R_2}{R_1}\frac{1+\frac{s_z}{s}}{1+\frac{s}{s_p}} \tag{10}$$

Using this configuration and assuming that C_2 is smaller than C_1, the poles and zeros are placed according to the following formulas:

$$f_{po} = f_z = \frac{1}{2\pi R_2 C_1} \tag{11}$$

$$f_p = \frac{1}{2\pi R_2 C_2} \tag{12}$$

$$G_0 = \frac{R_2}{R_1} \tag{13}$$

If we apply these expressions to the 43-° phase boost at 1 kHz associated with a 22-dB gain at the same frequency, we obtain the following component values, assuming R_1 is 10 kΩ:

C_1 = 2.35 nF
C_2 = 550 pF
R_1 = 10 kΩ
R_2 = 155 kΩ

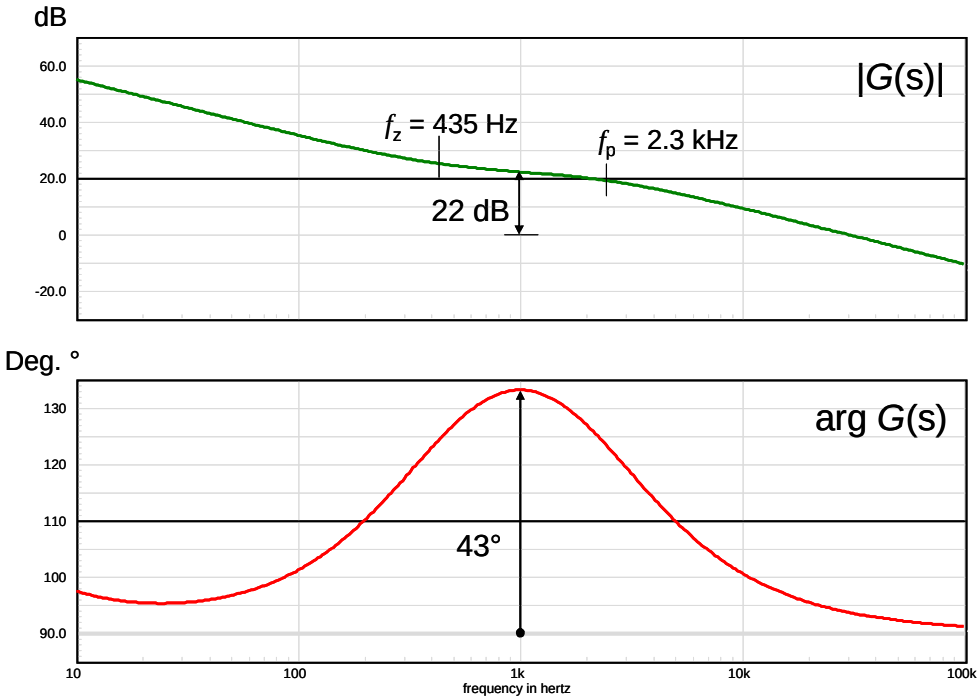

Figure 8: the transfer function reveals the right gain and phase boost we are looking for.

An ac simulation carried on Figure 7 schematic leads to the plot appearing in Figure 8. This drawing confirms the amplitudes on both the gain and phase we are looking for.

If the op amp is widely used in today electronic systems, it has been dethroned by the TL431 thanks to its cost and ease of implementation. However, because of its architecture, the TL431 requires a bit of care to implement a true type 2 compensator.

The type 2 with a TL431

Reference [2] details the presence of so-called fast and slow lanes which can appear troublesome when implementing the TL431. However, experience shows that using these lanes at your advantage actually makes the type 2 configuration an easy option as confirmed by Figure 9. The main trouble here is brought by the presence of the optocoupler. Its role is to convey the isolated secondary-side LED current, representative of the output voltage variation, to the primary section in direct electrical link to the mains. The bipolar transistor used to collect the photons emitted by the LED presents an internal collector-based capacitor directly proportional to the optocoupler Current Transfer Ratio (CTR). Because of the Miller effect, this capacitor multiplied by the transistor beta is seen on the collector and directly interacts with the pull-up or pull-down resistor connected to it. In certain cases, it can hamper the loop transfer function and care must be taken to account for its presence. The

larger the CTR, the larger the parasitic capacitor and the slower the optocoupler. The final transfer function appears in (14) where we can identify the following poles and zeros:

$$G(s) = -\left(\frac{sR_1C_1+1}{sR_1C_1}\right)\left(\frac{1}{1+sR_{pullup}\left(C_2 \| C_{opto}\right)}\right)\frac{R_{pullup}}{R_{LED}}CTR \tag{14}$$

$$f_z = f_{p0} = \frac{1}{2\pi R_1 C_1} \tag{15}$$

$$f_p = \frac{1}{2\pi R_{pullup}\left(C_2 \| C_{opto}\right)} \tag{16}$$

$$G_0 = \frac{R_{pullup}}{R_{LED}}\text{CTR} \tag{17}$$

In equation (14), C_{opto} is the equivalent optocoupler pole seen from the transistor collector which comes in parallel with Figure 9's C_2. As an immediate remark, if C_{opto} is small enough, implying a wide optocoupler bandwidth, its effect over C_2 will be negligible and C_2, alone, will dominate the pole position. On the opposite, depending on the crossover frequency selection, it can appear than the optocoupler parasitic capacitance imposes a pole lower than what equations (8) would suggest. In that case, C_2 has obviously no reason to exist and the optocoupler rules the position. In this particular case, either you select a wider-bandwidth optocoupler or you lower the crossover frequency until the final combination capacitance requires, at least, a C_2 capacitor value of 100 pF. This capacitor will be located closely to the PWM controller and will improve noise immunity.

Before running the type 2 components calculation, you absolutely need to know the optocoupler pole position. You can either characterize it yourself using the text fixture recommended in the optocoupler data sheet or look at the frequency response curves, usually dependent on the loading resistor. For a SFH615A-2 associated with a NCP1271 from ON Semiconductor, the cut-off frequency is 4.5 kHz and the CTR exhibits a poor value of 30% when connected to the controller 20-kΩ pull-up resistor. The equivalent collector-emitter capacitor is therefore:

$$C_{opto} = \frac{1}{2\pi \times 4.5k \times 20k} \approx 1.8\ nF \tag{18}$$

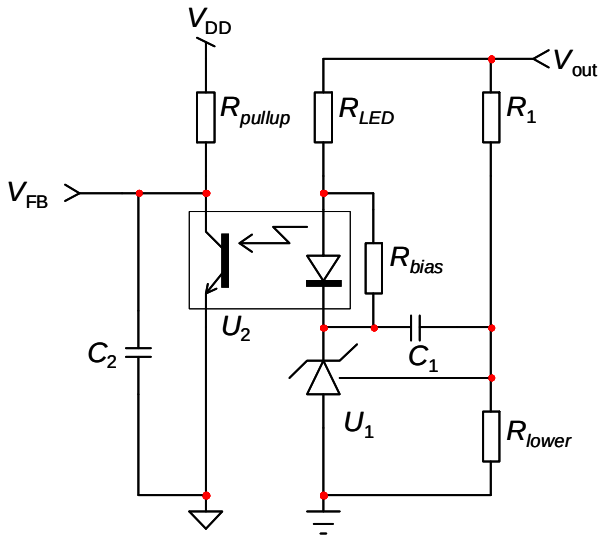

Figure 9: a complete return chain based on a TL431 and the optocoupler

From our previous example, we know that a zero must occur at 435 Hz and a pole at 2.3 kHz. Let us apply equations (15) through (17) to calculate the component values, still assuming R_1 is 10 kΩ:

$$C_1 = \frac{1}{2\pi R_1 f_z} = \frac{1}{6.28 \times 10k \times 435} \approx 37\ nF \tag{19}$$

$$C_{pole} = \frac{1}{2\pi f_p R_{pullup}} = \frac{1}{6.28 \times 2.3k \times 20k} \approx 3.5\ nF \tag{20}$$

However, C_{pole} is made of C_2 combined with C_{opto}. As C_{opto} is 1.8 nF, C_2 is simply:

$$C_2 = C_{pole} - C_{opto} = 3.5n - 1.8n = 1.7\ nF \tag{21}$$

Finally, the LED series resistor characterizes the mid-band gain necessary to cross over at the selected 1-kHz frequency. From (17), we have:

$$R_{LED} = \frac{R_{pullup}\text{CTR}}{G_0} = \frac{20k \times 0.3}{10^{\frac{22}{20}}} = 476\ \Omega \tag{22}$$

The extra resistor, R_{bias}, ensures the circulation of a certain amount of current in the TL431. Adopting a value of 1 kΩ makes the adjustable reference operate as per the data-sheet recommendations which state a 1-mA minimum bias current.

Simulating the TL431 network

Before building the breadboard in the bench, it is good to test the frequency response on the computer first. This is what Figure 10 proposes, using a SPICE simulator like Intusoft's IsSpice. In this particular case, we have added an automatic bias control to force the optocoupler collector to operate at 2.5 V, otherwise stated, in the middle of its dynamic excursion. Given the high gain of the TL431, manually setting the bias point by tweaking its input dc bias (actually the regulated V_{out} in the real application) would certainly complicate the task. This function is performed by E_1 and the loop opening elements like *CoL* and *LoL*: *LoL* is a short-circuit during the bias point calculation (dc analysis) while *CoL* is open. In ac, *LoL* is very large and is considered as open, therefore, all the ac signal can flow via *CoL* without being bothered by E_1. A similar configuration can be used to test the dc gain of an operational amplifier for instance.

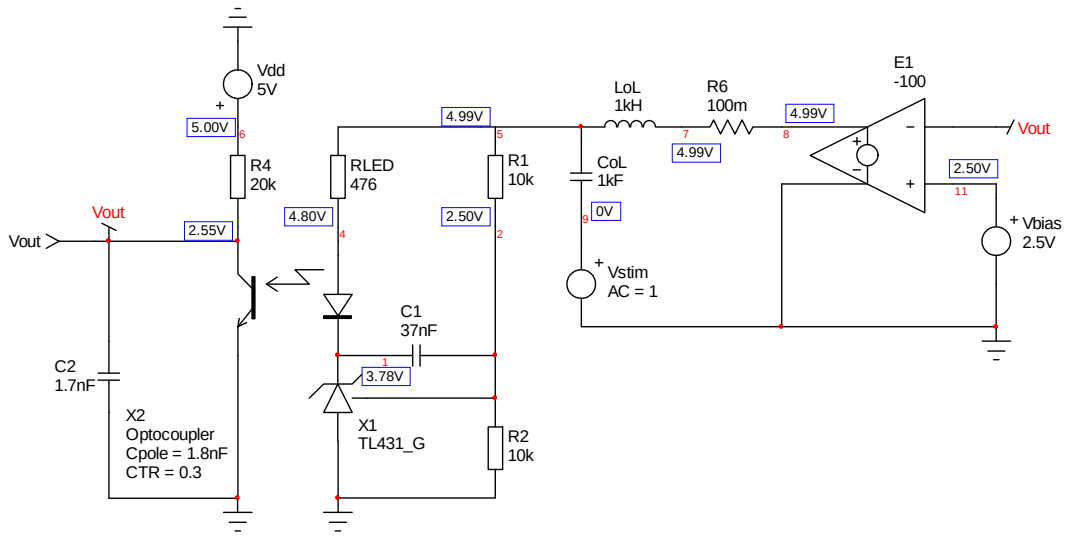

Figure 10: a simple simulation fixture helps to test the type-2 amplifier built around the TL431.

The bias resistor has been omitted as the generic TL431 SPICE model we used is not sensitive to its bias current value. The final results appear in Figure 11.

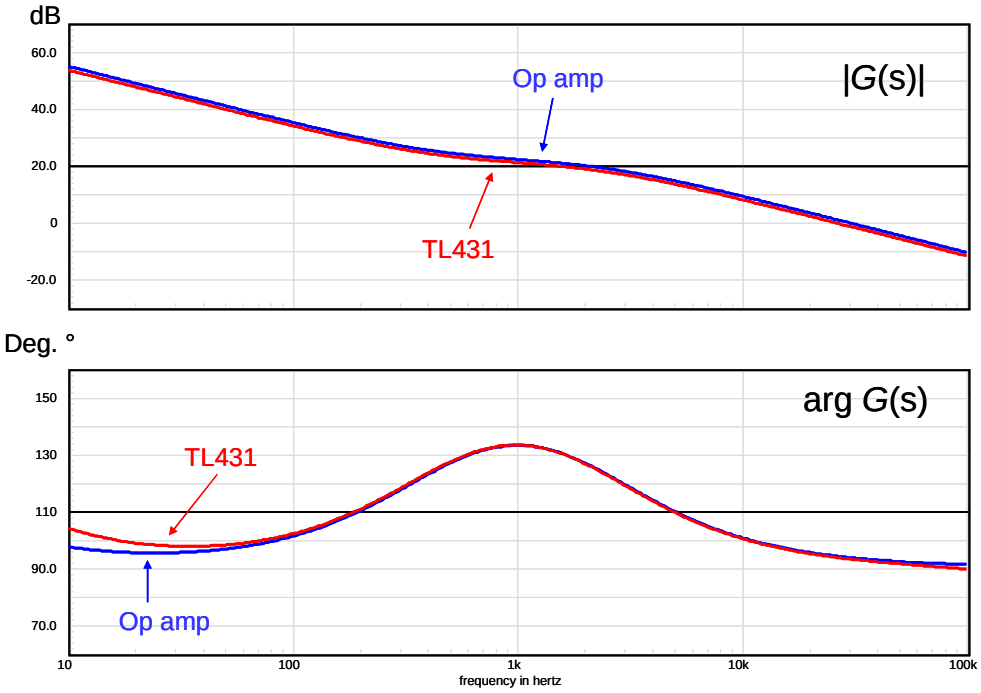

Figure 11: the ac results delivered by the TL431 arrangement fit very well the op-amp-based type 2 reference.

The TL431 ac response agrees very well with that of the op-amp-based type 2 compensator. We can however notice a small difference in the developed gain at the 1-kHz crossover frequency. This 1-dB discrepancy is imputed to the LED dynamic resistor R_d which appears in series with R_{LED}. This dynamic resistance depends on the LED direct current I_F which is indirectly linked to the collector pull-up resistor. For low bias currents, as in our example, ≈ 300 µA, this dynamic resistor can easily reach 150 Ω whereas it drops to 40 Ω when operated at higher currents like 1 mA. Therefore, depending on the LED series resistor, this dynamic resistor can have a small impact on the mid-band gain. If you would now add the 1-kΩ bias resistor in parallel with the optocoupler LED, you would notice a further gain reduction, again, imputable to the rather high R_d value from which the extra bias resistor steals away feedback current. These effects are almost invisible at higher LED forward currents, i.e. with optocoupler operating currents in the vicinity of 1 mA or more. As a temporary conclusion, selecting pull-up resistors in the 1-5 kΩ range helps to a) widen the optocoupler bandwidth b) to cancel the LED dynamic resistor impact c) improve the optocoupler current transfer ratio. The cons against these choices are the power consumed in no-load operation as the internal pull-up resistor draws current when the optocoupler imposes a low V_{CE} voltage. When you chase every tens of mW to draw less than 100 mW at a 230-V-rms input line, these little details have their importance!

Watch the LED series resistor value

There is another important comment regarding the series resistor R_{LED}. As shown by (22), it plays a role in the mid-band gain and must be calculated with care (no trial and error, please!). However, this equation alone is not enough to end the design phase. The series resistor also limits the current excursion in the optocoupler LED. In our case, the maximum current authorized by the 476-Ω resistor would be:

$$I_{LED,\max} = \frac{V_{out} - V_f - V_{TL431,\min}}{R_{LED}} = \frac{5-1-2.5}{476} = 3.15\,mA \tag{23}$$

This current reflected to the optocoupler collector via its CTR turns into the following value:

$$I_{C,\max} = I_{LED,\max}\mathrm{CTR}_{\min} = 3.15\times 0.3 = 945\,\mu A \tag{24}$$

Given the 20-kΩ pull-up resistor, this current is large enough to pull the collector voltage down as the feedback loop instructs in light load conditions. The situation obviously worsens if you try to compensate a converter delivering a voltage lower than 5 V, e.g. 3.3 V. In this case, a TLV431 could be a better choice as its voltage can go down to 1.24 V. Based on these observations, we can derive another equation imposing a limit on the R_{LED} choice:

$$R_{LED,\max} \le \frac{V_{out} - V_f - V_{TL431,\min}}{V_{dd} - V_{CE,sat}} R_{pullup} \mathrm{CTR}_{\min} \le \frac{5-1-2.5}{5-0.3} \times 0.3 \times 20k \le 1.91\, k\Omega \qquad (25)$$

If you decide to provide the extra 1-mA bias to the TL431 by paralleling a 1-kΩ resistor across the optocoupler LED, the above equation must be updated since this current also crosses the LED series resistor:

$$R_{LED,\max} \le \frac{V_{out} - V_f - V_{TL431,\min}}{V_{dd} - V_{CE,sat} + I_{bias} \mathrm{CTR}_{\min} R_{pullup}} R_{pullup} \mathrm{CTR}_{\min} \le \frac{5-1-2.5}{5-0.3+1m \times 0.3 \times 20k} \times 0.3 \times 20k \le 841\,\Omega \qquad (26)$$

In the above equations, we have:

V_{out}, the output voltage
I_{bias}, the TL431 biasing current when the optocupler LED is paralleled with a resistor (usually 1 kΩ for a 1-mA bias)
$V_{TL431,min}$, the minimum voltage the TL431 can go down to (2.5 V)
V_f, the optocoupler LED forward drop (≈ 1 V)
CTR_{min}, the minimum optocoupler current transfer ratio
$V_{CE,sat}$, the optocoupler saturation voltage (≈ 300 mV at a 1-mA collector current)
V_{dd}, the internal bias of the pull-up resistor

As a result, the minimum gain brought by a 20-kΩ pull-up resistor in a TL431-based feedback network using an optocoupler affected by a 30% CTR is:

$$G_0 \ge \frac{R_{pullup}}{R_{LED,\max}} \mathrm{CTR}_{\min} \ge \frac{V_{dd} - V_{CE,sat}}{V_{out} - V_f - V_{TL431,\min}} \ge 3.13 \text{ or } \approx 10\ dB \qquad (27)$$

If we consider (26), this gain even goes up to 17 dB! This is the major drawback of a feedback control operated with a TL431 in a type 2 arrangement. It naturally offers less flexibility than a traditional op-amp-based type 2 compensator where the mid-band gain can be adjusted at any value. Assume that Figure 6 reveals a gain deficiency of -5 dB at 1 kHz, you could simply not use the arrangement featuring the 20-kΩ pull-up resistor to create a mid-band gain of +5 dB at 1 kHz. This is because the origin pole and the zero are linked by a coefficient made of the CTR, the pull-up and the LED resistors. The only solution is to select a different crossover frequency where the gain deficiency is compatible with the limitations described by equations (25) and (27) or to go for a type 1 compensator, provided no phase boost is necessary.

Final result

The TL431 compensator has been installed on the CCM flyback and the loop gain *T(s)* has been plotted in Figure 12. As you can see, the crossover frequency is 1 kHz and the phase margin reflects exactly what we were looking for: 70°. These are simulation results and the next step is to build the prototype and make sure through bench measurements that experiments confirm the choices we have made.

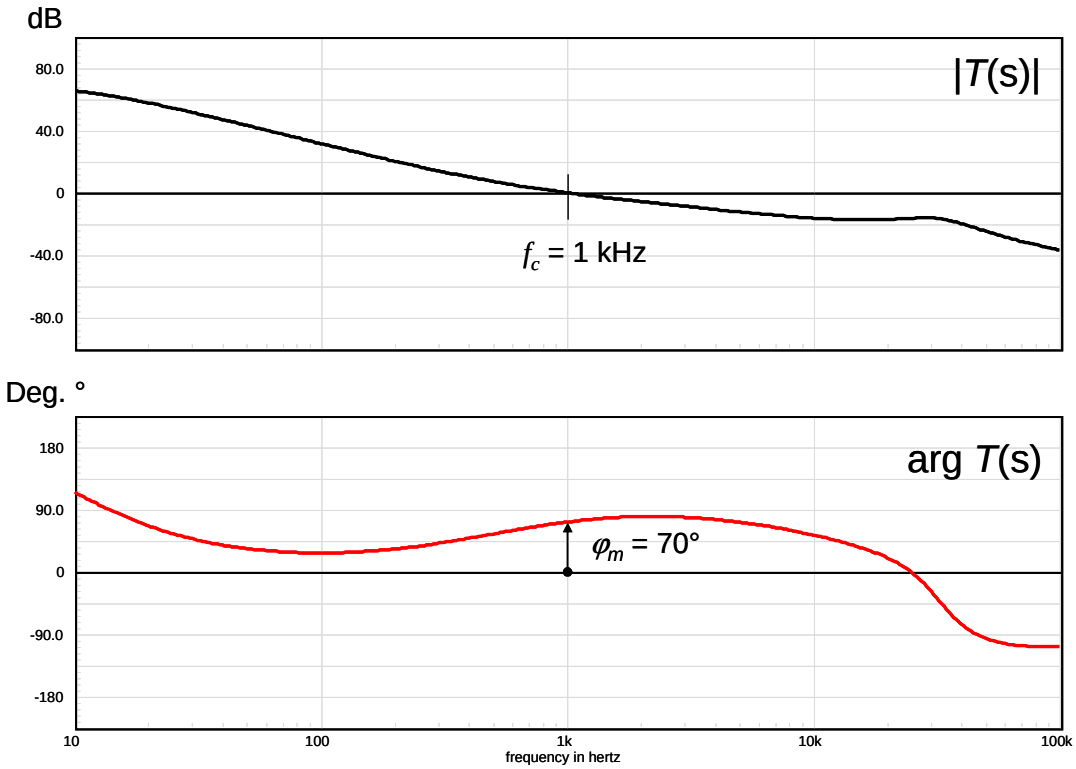

Figure 12: the CCM flyback converter loop gain confirms the 1-kHz crossover frequency and the adequate phase margin.

Conclusion

The TL431 lends itself very well to the type 2 implementation. It is however important to understand the limitations brought by the configuration. For instance, in cases where a reduced gain is needed in the mid-band area, the designer might be forced to chose a different crossover frequency where the gain conditions are more favorable. Despite these little drawbacks, the TL431 implemented in a feedback loop is still the most popular choice in consumer power supplies.

References

1. C. Basso, “Eliminate the guesswork in crossover frequency selection”, Power Electronics and Technology, August 2008
2. C. Basso, “Switch Mode Power Supplies: SPICE Simulations and Practical Designs”, McGraw-Hill, 2008
3. C. Basso, “Transient response counts when choosing phase margin”, Power Electronics and Technology, November 2008

The TL431 in Switch-Mode Power Supplies loops: part III

Christophe Basso – ON Semiconductor
14, rue Paul Mesplé – BP53512 - 31035 TOULOUSE Cedex 1 - France

In a previous article, we have showed how to implement a type 2 compensator using a TL431. Unfortunately, the TL431 does not represent a panacea in terms of compensation circuit. As the origin pole and the zero are linked by a fixed coefficient, you loose the flexibility naturally inherent to a compensator built around an operational amplifier (op amp) where you can create the mid-band gain of your choice. To solve the case where the LED series resistor clamps the possible gain variations, a type 1 compensator will offer the flexibility we are looking for when stabilizing the converter of our choice. However, the type 1 also suffers from one limitation: it does not offer any phase boost.

Understanding the limitation of a TL431-based type 2 compensator

A type 2 compensator using a TL431 appears in Figure 13 and creates a pole at the origin, f_{po}, a pole f_p and finally, a zero f_z. The equation describing a type 2 compensator made with a TL431 appears in (1) and shows the presence of a combined action of the optocoupler parasitic capacitance C_{opto} with the added capacitor C_2.

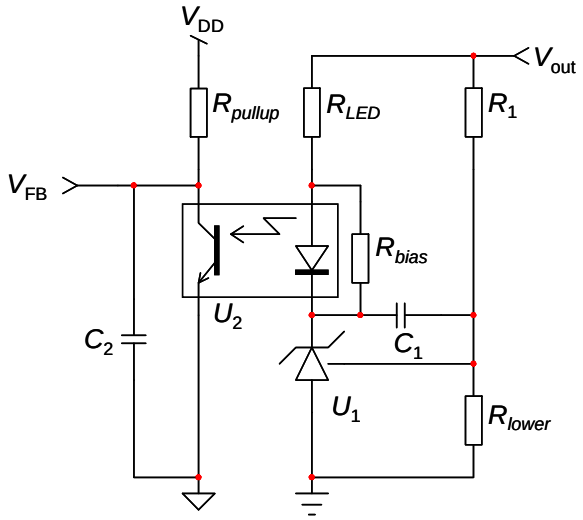

Figure 13: a type 2 compensator built around a TL431.

$$G(s) = -\left(\frac{sR_1C_1 + 1}{s\dfrac{R_1R_{LED}}{R_{pullup}\mathrm{CTR}}C_1}\right)\left(\frac{1}{1 + sR_{pullup}\left(C_2 \,\|\, C_{opto}\right)}\right) \tag{1}$$

From this equation, we can extract the following poles and zero definitions:

$$f_{po} = \frac{1}{2\pi\dfrac{R_1R_{LED}}{R_{pullup}\mathrm{CTR}}C_1} \tag{2}$$

$$f_z = \frac{1}{2\pi R_1C_1} \tag{3}$$

$$f_p = \frac{1}{2\pi R_{pullup} C_{pole}} = \frac{1}{2\pi R_{pullup} \left(C_2 \left\| C_{opto} \right. \right)} \tag{4}$$

When dividing equation (2) and (3), we can see a link between the origin pole and the zero:

$$\frac{f_{po}}{f_z} = G_0 = \frac{R_{pullup} \text{CTR}}{R_{LED}} \tag{5}$$

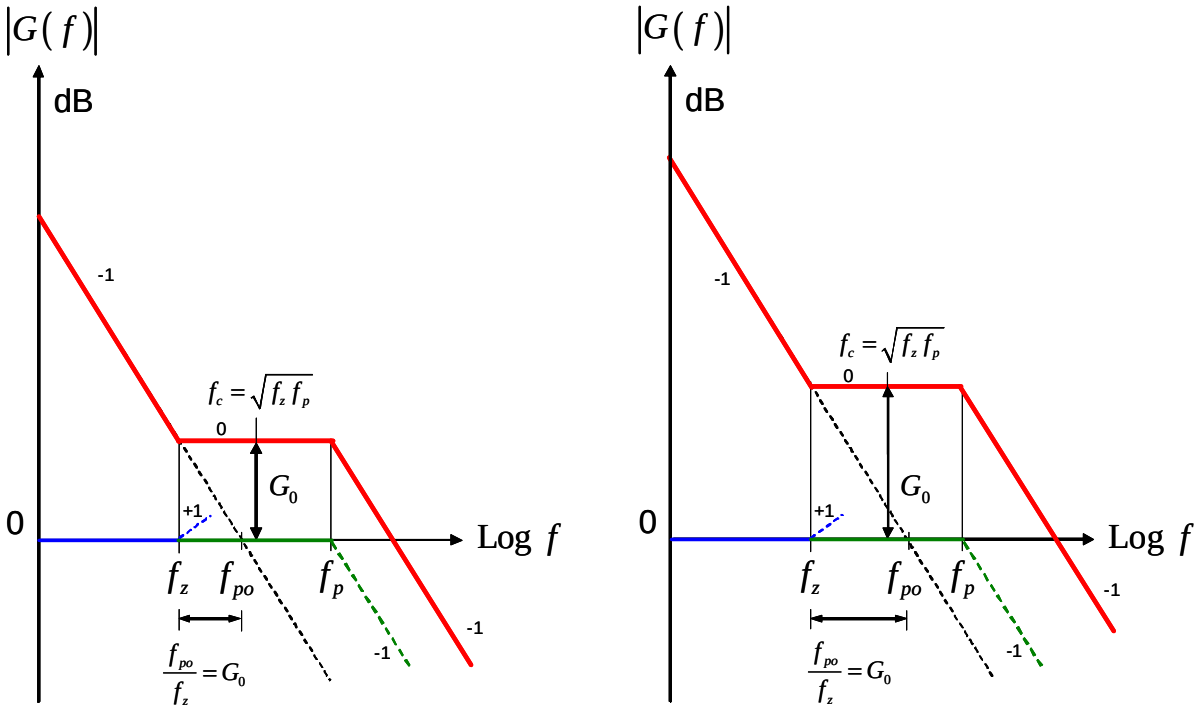

Figure 14: by adjusting the distance between the origin pole and the zero, the mid-band gain is selected.

As the zero is fixed and depends upon the upper resistor R_1 and C_1 (3), adjusting the LED series resistor R_{LED} gives us a means to change the origin pole position (2). By doing so, we can easily tweak the mid-band gain to the desired value. This is what Figure 14 displays, showing how two different origin pole positions alter the mid-band gain G_0. However, the freedom to increase the LED resistor is limited by the necessary current excursion in the optocoupler collector. We can show that the LED series resistor cannot exceed the following value:

$$R_{LED,\max} \le \frac{V_{out} - V_f - V_{TL431,\min}}{V_{dd} - V_{CE,sat}} R_{pullup} \text{CTR}_{\min} \tag{6}$$

If you decide to provide the extra 1-mA bias to the TL431 by paralleling a 1-kΩ resistor across the optocoupler LED, as drawn in Figure 13, the above equation must be updated since this current also crosses the LED series resistor:

$$R_{LED,\max} \le \frac{V_{out} - V_f - V_{TL431,\min}}{V_{dd} - V_{CE,sat} + I_{bias} \text{CTR}_{\min} R_{pullup}} R_{pullup} \text{CTR}_{\min} \tag{7}$$

Where:

V_{out}, the output voltage

I_{bias}, the TL431 biasing current when the optocupler LED is paralleled with a resistor (usually 1 k Ω for a 1-mA bias)
$V_{TL431,min}$, the minimum voltage the TL431 can go down to (2.5 V)
V_f, the optocoupler LED forward drop (≈ 1 V)
CTR_{min}, the minimum optocoupler current transfer ratio (30% for a SHF615-2 at a 350-µA collector current)
$V_{CE,sat}$, the optocoupler saturation voltage (≈ 300 mV at a 1-mA collector current) which imposes the minimum feedback voltage.
V_{dd}, the internal bias of the pull-up resistor, usually 5 V

Substituting (6) in (5), gives the minimum mid-band gain that a type 2 compensator using a TL431 can achieve:

$$G_0 \geq \frac{R_{pullup}}{R_{LED,\max}}\mathrm{CTR}_{\min} \geq \frac{V_{dd}-V_{CE,sat}}{V_{out}-V_f-V_{TL431,\min}} \tag{8}$$

In the case of a 5-V converter and using the above values, this mid-band gain could not be made lower than ≈10 dB. This situation would even worsen if equation (7) was used to calculate R_{LED}. What are the implications of such a limit? The compensation technique that we adopt implies a shift on the power stage gain curve *H(s)* up or down by a certain amount of gain (or attenuation) in order to force the 0-dB crossover at a selected frequency. A type 2 compensator based on an op amp offers enough design freedom in the selection of the surrounding elements to let you amplify or attenuate the power stage gain curve at the crossover frequency. On the contrary, (8) poses a rather stringent design limit when the selected crossover frequency concerns a point on the gain curve where a limited gain - or even worse, an attenuation - is concerned. Suppose the selected crossover point on the power stage gain curve exhibits a magnitude of -5 dB. To crossover at this very point, you would need to shift the whole curve by +5 dB at the selected frequency. Unfortunately, the 10-dB minimum gain limit imposed by (8) would prevent you from reaching this goal and there is nothing you could do against that. The case further worsens in presence of a large gain excess at the crossover frequency, in case of a Power Factor Corrector, for instance. How do we do then? Well, either you select the crossover frequency in a different region where the needed mid-band gain complies with (8) or, you identify a region where no phase boost is necessary. With this option, a simple type 1 can do the job. In this case, because the mid-band gain parameter disappears, we can adopt a different calculation strategy for the TL431.

A type 1 compensator with the TL431

The schematic does not differ from that of Figure 13 and (1) is obviously still valid. However, to perform an integration function and keep the origin pole alone, we have to make the upper pole and the zero coincident. Then, we select the LED resistor to a value compatible with the result given by (6). The difference with the type 2 derivation lies in the upfront selection of the LED resistor. For a 5-V output and considering a 1-mA bias provided the way Figure 13 suggests, we can calculate the maximum value this resistor can take using (7):

$$R_{LED,\max} \leq \frac{5-1-2.5}{5-0.3+1m\times 0.3\times 20k}\times 0.3\times 20k \leq 841\,\Omega \tag{9}$$

Adopting a 50-% margin on the result, we could fix the R_{LED} resistor to 420 Ω or 470 Ω for the normalized value. Knowing that both the zero and the pole are coincident, we have (3) equal to (4) from which we can extract the zero capacitor value:

$$C_1 = C_{pole}\frac{R_{pullup}}{R_1} \tag{10}$$

Replacing C_1 in (2) by (10), we obtain the definition for the pole capacitor made of the capacitor C_2 in parallel with the parasitic capacitor of the optocoupler C_{opto}:

$$C_{pole} = \frac{\mathrm{CTR}}{2\pi f_{po} R_{LED}} \tag{11}$$

The origin pole location must now be selected so that the attenuation G_{fc} at the crossover frequency f_c exactly compensates the excess or deficiency of gain read on the power stage Bode plot. An origin pole transfer function follows equation (12) in which ω_{po} represents the origin pole:

$$G(s) = \frac{1}{\frac{s}{\omega_{po}}} \tag{12}$$

From the above equation, we can calculate the magnitude of *G(s)* at the crossover frequency:

$$|G(f_c)| = \frac{f_{po}}{f_c} \tag{13}$$

We can now extract the origin pole location and feed (11) to get C_{pole}:

$$f_{po} = G_{f_c} f_c \tag{14}$$

Once C_{pole} is known, we obtain C_1 using (10).

Application example

To illustrate a type 1 design, we have selected a single-stage PFC using a flyback structure delivering a 12-V output voltage. The circuit uses a borderline controller like the MC33262 from ON Semiconductor. This controller operates in peak current mode control but a NCP1606 implementing a voltage-mode architecture would give similar results: both would operate in fixed on-time. Figure 15 portrays the application schematic built around the auto-toggling current-mode models studied in Ref. [1]. The peak current set point is actually elaborated by modulating the amplitude of the rectified full-wave signal available on the upper terminal of R_1 by the error signal appearing on the optocoupler collector. The output voltage is 12 V, as expected, and it delivers 100 W from a 100-V rms input voltage. The displayed bias points confirm the proper dc point calculation.

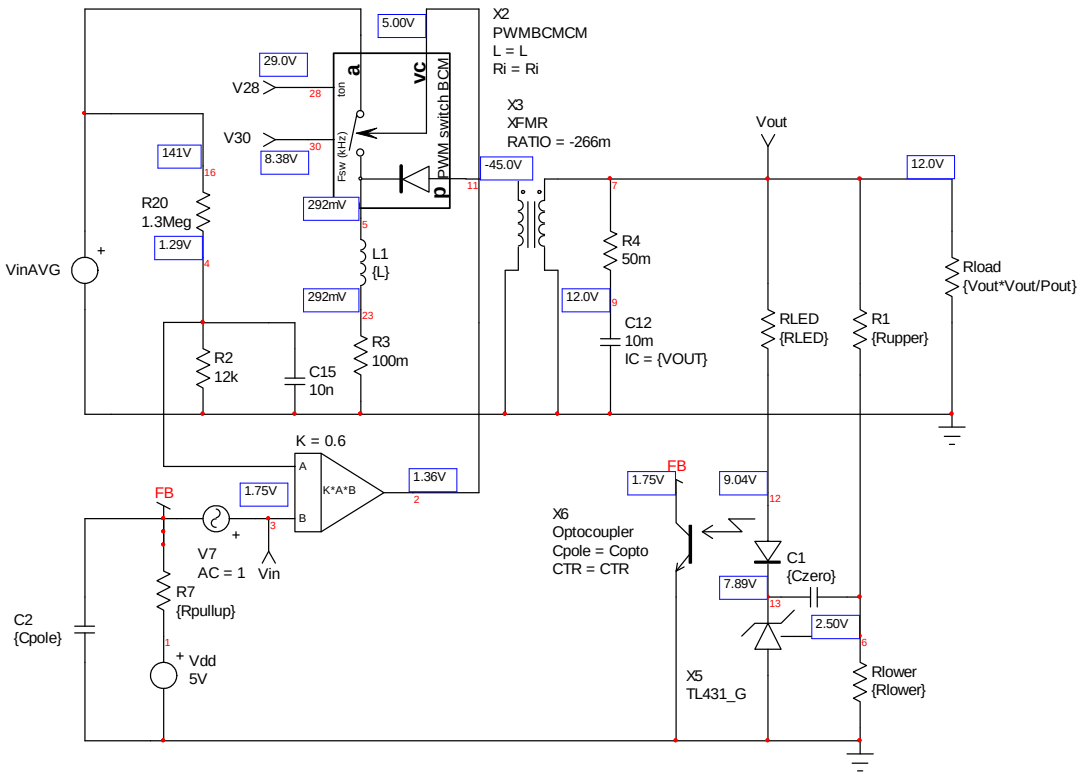

Figure 15: a single-stage PFC-flyback using a current-mode borderline controller such as the MC33262.

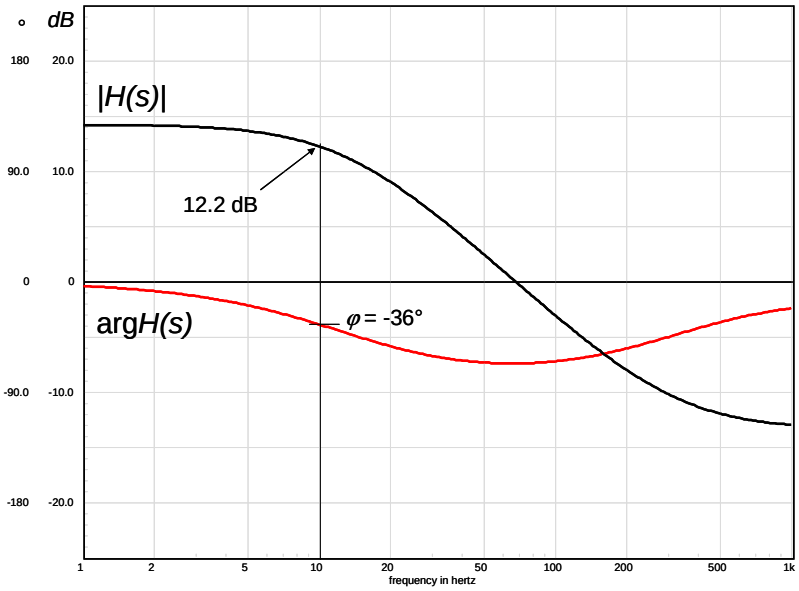

Figure 16: the power stage Bode plot shows a gain excess of 12.2 dB when operated from a 100-V rms input voltage.

The loop stability study starts with the power stage Bode plot which appears in Figure 16. This plot can either be generated manually using analytic analysis or by using a SPICE simulator as we did. Since we deal with a type 1 compensator, there is no added phase boost at the crossover point. Keeping a phase margin greater or equal to 45° naturally restricts the possible crossover frequency to ≈15 Hz where the power stage phase rotation starts to exceed 45°. At 10 Hz, the rotation is -36° and the excess gain reaches 12.2 dB. Using (8) in a classical type 2 configuration featuring a 12-V output, we could not pull down the gain curve beyond a minimum of -5 dB, whereas, in this example, we need to bring it down by -12.2 dB at 10 Hz: the type 1 compensator is mandatory in this case. Let us go through the calculation steps:

1. evaluate the maximum allowable LED resistor with (7) :

$$R_{LED,\max} \le \frac{12-1-2.5}{5-0.3+1m\times 0.3\times 20k}\times 0.3\times 20k \le 4.76\ k\Omega \tag{15}$$

We will adopt a 2.2-kΩ resistor, leading to a comfortable safety margin.

2. calculate the needed attenuation at a 10-Hz crossover frequency:

$$G_{f_c} = 10^{\frac{-12.2}{20}} = 0.245 \tag{16}$$

3. position the origin pole:

$$f_{po} = f_c G_{fc} = 10\times 0.245 = 2.45\ Hz \tag{17}$$

4. with a 250-µA divider bridge current I_{bias} (good trade-off between noise immunity and standby power performance), calculate the upper and lower resistors:

$$R_{lower} = \frac{2.5}{250u} = 10\ k\Omega \tag{18}$$

$$R_1 = \frac{V_{out} - V_{ref}}{I_{bias}} = \frac{12 - 2.5}{250u} = 38\ k\Omega \tag{19}$$

With V_{ref} the TL431 internal reference voltage.

5. Calculate the required pole capacitor value:

$$C_{pole} = \frac{\text{CTR}}{2\pi f_{po} R_{LED}} = \frac{0.3}{6.28 \times 2.45 \times 2.2k} = 8.86\ \mu F \tag{20}$$

Knowing the optocoupler parasitic capacitor C_{opto} (assume you have characterized/extracted it to 2 nF) evaluate the added capacitor value C_2. Given the result given by (20), the optocoupler pole has no influence in this particular case:

$$C_2 = C_{pole} - C_{opto} \approx 8.86\ \mu F \tag{21}$$

A 10-µF electrolytic capacitor will be used for this purpose.

6. From the above value, evaluate the zero capacitor value:

$$C_1 = C_{pole} \frac{R_{pullup}}{R_1} = 10u \frac{20k}{38k} \approx 5.2\ \mu F \tag{22}$$

A 4.7-µF electrolytic capacitor will be selected for this function.

We have plugged these values into Figure 15 components and we obtained in Figure 17 the loop gain plot *T(s)*. The 10-Hz crossover is respected together with a 55-° phase margin. Thanks to the average model simulation speed, it is quick to simulate a start-up sequence and check the input current once the output is stabilized. Both waveforms appear in Figure 18. The output does not overshoot and exhibits a rather large ripple defined in [1]:

$$\Delta V = \frac{P_{out}}{2\pi F_{line} V_{out} C_{out}} = \frac{100}{6.28 \times 50 \times 12 \times 10m} \approx 2.6\ V_{pp} \tag{23}$$

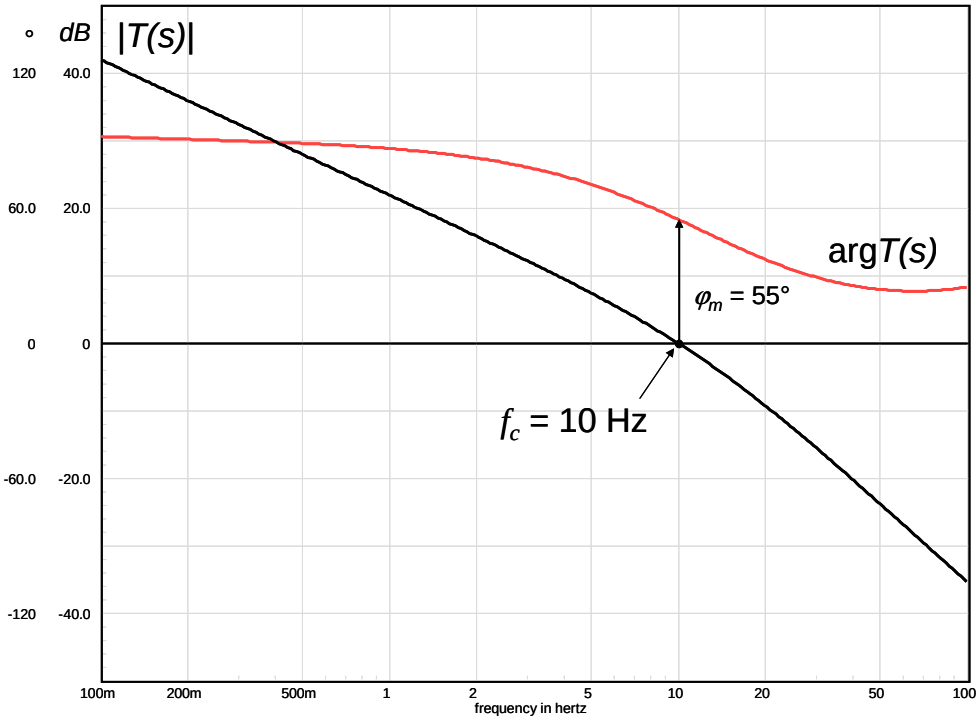

Figure 17: once compensated, the crossover frequency reaches the expected 10 Hz.

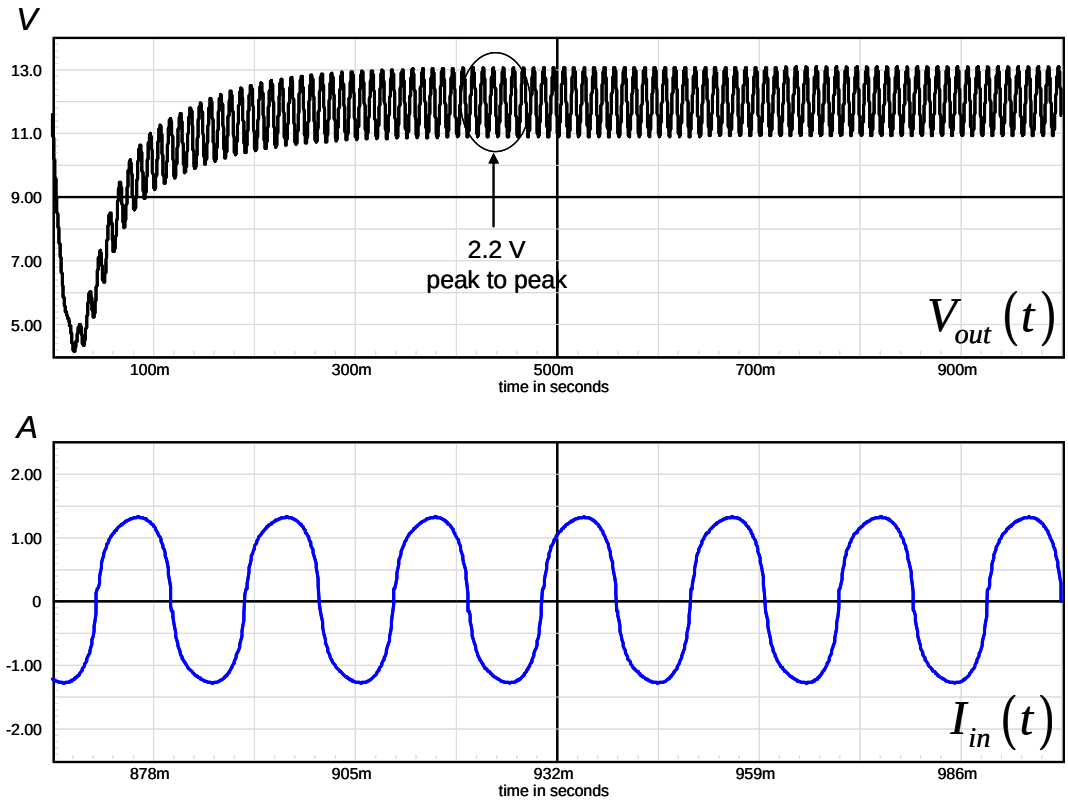

Figure 18: the transient response of the single-stage PFC flyback converter. The output ripple is typical of this structure.

The simulation shows a slightly less ripple amplitude however. The power factor is measured to 0.963, typical of this kind of architecture.

Conclusion

The TL431 in a type-2 configuration clamps down the minimum achievable gain and cannot be used in situation where a gain in excess needs to be compensated. In cases where no phase boost is necessary, the TL431 compensator can be re-arranged in a real type-1 application where the origin pole can be placed to cross over any frequency as we have showed in this article.

References

1. C. Basso, “Switch Mode Power Supplies: SPICE Simulations and Practical Designs”, McGraw-Hill, 2008

The TL431 in Switch-Mode Power Supplies loops: part IV

Christophe Basso – ON Semiconductor
14, rue Paul Mesplé – BP53512 - 31035 TOULOUSE Cedex 1 - France

In a previous series of articles, we have shown how the TL431 could be used to realize type 1 and type 2 kinds of compensators. If the aforementioned compensator types work with most of the current-mode control configurations, other control modes can require a type 3. For instance, if you have to compensate a continuous conduction mode (CCM) voltage-mode converter, you need an extra pole and zero. In this configuration, the TL431 does not lend itself very well to this exercise: the fast lane presence clearly complicates the design task. The simple idea developed in this article consists in getting rid of the fast lane via an external dc bias, fully decoupled from the observed ac input. In that particular case, the design exercise nicely simplifies and resembles that of a classical type 3 built upon an operational amplifier.

The type 3 implemented with the TL431

A type 3 compensator using a TL431 appears in Figure 19. It creates a pole at the origin, f_{po}, two poles f_{p1} and f_{p2}, plus two zeros, f_{z1} and f_{z2}. Thanks to this configuration, the designer can boost the phase at the crossover frequency up to a theoretical limit of 180°.

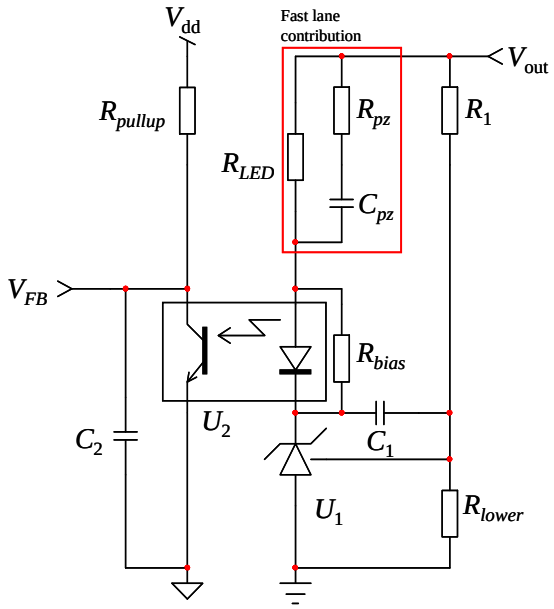

Figure 19: a type 3 built around a TL431 is hampered by the presence of the fast lane which introduces an extra modulation via R_{LED}.

Unfortunately, as derived in Ref. [1], the LED resistor, in this particular arrangement, plays two roles: one for the mid-band gain and the second one for the extra zero position. This is what the following transfer function confirms:

$$\frac{V_{FB}(s)}{V_{out}(s)} = -\frac{R_{pullup}}{R_{LED}}\,\mathrm{CTR}\,\frac{(sR_1C_1+1)\left[s\left(R_{LED}+R_{pz}\right)C_{pz}+1\right]}{sR_1C_1\left(1+sR_{pullup}C_2\right)\left(sR_{pz}C_{pz}+1\right)} \tag{1}$$

Therefore, finding the right combination where R_{LED} gives the correct gain but also the required zero position, still making sure R_{LED} satisfies the minimum biasing conditions… you have understood it, the exercise is a nightmare! The reason for this situation? The presence of the fast lane which routes a portion of the output voltage in parallel with the voltage divider made of R_1 and R_{lower}. If R_{LED} was solely used to dc bias purposes, without an ac connection to the input voltage V_{out}, it would certainly disappear from any pole/zero combination present in (1).

The fast lane is the problem

The problem comes from the connection of R_{LED} to the input signal, V_{out}. In a classical op amp-based configuration, the input modulation is solely conveyed to the output by the resistors bridge R_1 and R_{lower} sensing V_{out}. In the TL431 case, because of its connection to V_{out}, R_{LED} also appears in the modulation path and plays a role in the transfer function. When C_1 is a short circuit, i.e. at high frequencies, the transmission of the V_{out} modulation to the LED via the resistor bridge disappears and the TL431 becomes a simple Zener diode, fixing the LED cathode potential. However, because of the link to V_{out} via R_{LED}, the modulation still reaches the LED and thus V_{FB}, by affecting the optocoupler current as follows:

$$I_L(s) = \frac{V_{out}(s)}{R_{LED}} \tag{2}$$

The equivalent schematic appears in Figure 20 where, despite the absence of link between R_1/R_{lower} and U_1 (because C_1 acts as a short-circuit), a modulated current crossing R_{LED} alone reaches the output as shown on the right hand side of the picture. This particular configuration makes the design of a type 3 a difficult exercise, as (1) can justify.

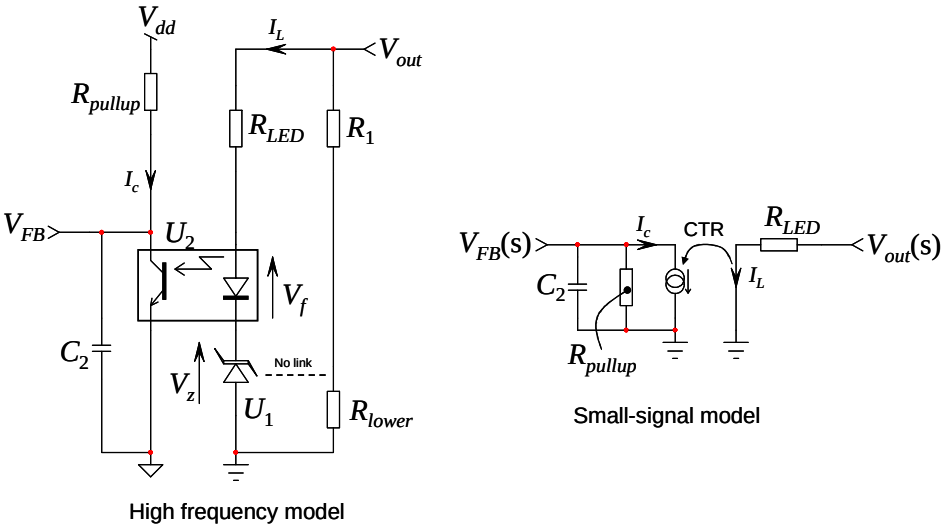

Figure 20: as the feedback capacitor C_1 becomes a short circuit at high frequencies, the LED cathode potential is fixed by the TL431 and a modulated current still reaches the optocoupler via the series resistor R_{LED}.

An open-collector operational amplifier

The fast lane creates the problem because of its connection to V_{out}. To get rid of this situation, the best way is to connect the R_{LED} resistor to a fixed potential, fully decoupled from V_{out}. There are several options to reach this goal, but the simplest one is to use a Zener diode as portrayed by Figure 21 which depicts a type 2 compensator (1 pole at the origin, a low frequency zero and a high frequency pole). In this application schematic, a portion of the output current is derived via resistor R_3 to bias both a Zener diode D_z and the TL431. Thanks to the presence of D_Z, C_Z and R_Z the bias node becomes insensitive to the ac modulation appearing on the output voltage. Of course, sufficient headroom between the output voltage and the selected Zener voltage must exist to guaranty the needed ac isolation. For a 12-V output, a 6.2-V Zener has proven to be a good choice. Select Zener diodes accepting a moderate bias current to avoid pumping out unnecessary static current from the regulated output, especially if no-load standby power is a requirement. The MM3Z6V8ST1 from ON Semiconductor could be a pertinent choice given the low breakdown current at which they are specified. The resistor R_z is calculated to include the Zener diode bias current but also the optocoupler current associated with the 1-mA minimum requirement for the TL431 operation. We will come back on R_z in the design examples below.

Now that the fast lane contribution has disappeared, we are left with a classical open-collector operational amplifier configuration where all the calculation rules available for types 2 and 3 readily apply. The TL431 is made of an op amp whose non inverting input is biased to 2.5 V. The voltage output of this op amp is actually seen at the TL431 cathode, on the node denominated *k* in Figure 21. The ac current crossing the LED is therefore the voltage at node *k*, divided by the series resistor R_{LED} (see Figure 20 for the small-signal model where V_{out} is simply replaced by *V(k)*)

$$I_L(s) = \frac{V_k(s)}{R_{LED}} \tag{3}$$

The current I_c circulating in the optocoupler collector is linked to that of the LED by the Current Transfer Ratio or CTR:

$$I_c(s) = I_L(s)\,\mathrm{CTR} \tag{4}$$

Since this current circulates in the pull-up resistor to create the output voltage, we have:

$$V_{FB}(s) = R_{pullup} I_c(s) \tag{5}$$

From the above equations, it is easy to extract the dc gain G_0 brought by this added circuit to the TL431 op amp output:

$$\frac{V_{FB}(0)}{V_k(0)} = G_0(0) = \frac{R_{pullup}}{R_{LED}}\mathrm{CTR} \tag{6}$$

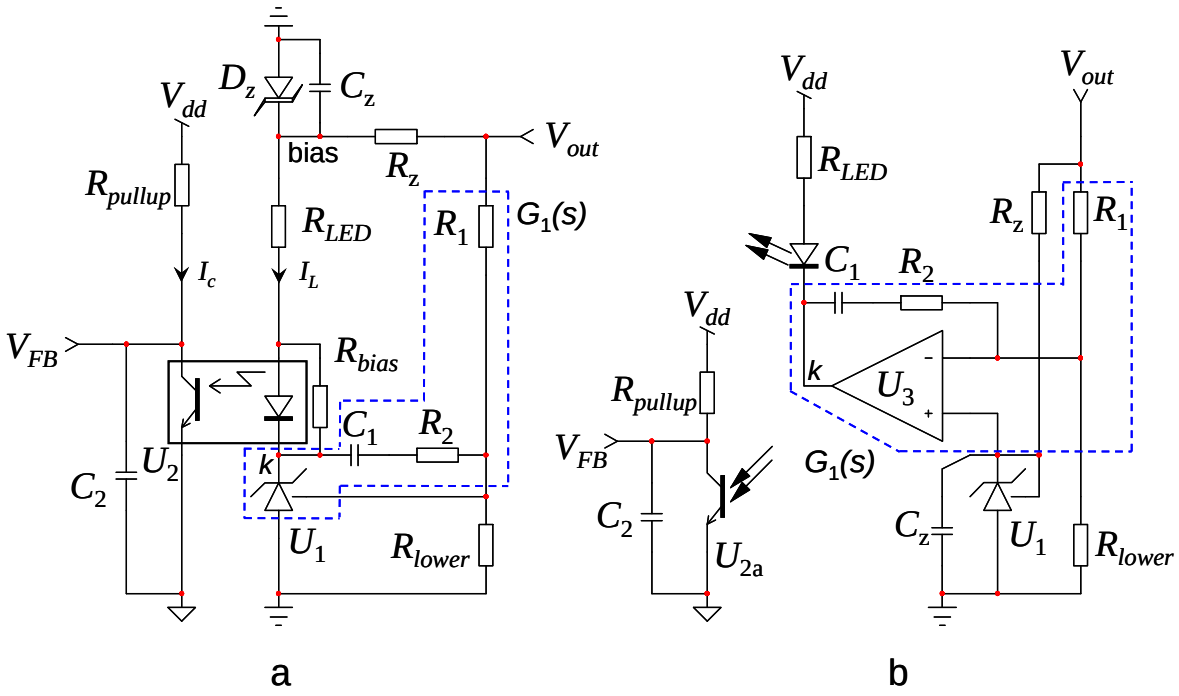

Figure 21a and b: a Zener diode can be used to create a fixed dc level, further decoupled from the monitored output voltage by a capacitor as shown on sketch a. On side b, despite the presence of an op amp, the way the information is conveyed on the primary side does not differ: it has to cross the optocoupler imposing its pole and CTR.

In ac, remember that the optocoupler, by its physical constitution, is limited in response time. This fact can be modeled by considering a parasitic capacitor, C_{opto}, placed between its collector-emitter terminals. As a result, a capacitor made of $C_2 \parallel C_{opto}$ connected to the optocoupler collector introduces a high frequency pole. In other words, whatever the way V_{out} is shaped in magnitude and phase by the TL431, the voltage delivered on node *k* will undergo the following ac expression, involving the dc gain already derived in (6):

$$\frac{V_{FB}(s)}{V_k(s)} = G_0(s) = \frac{R_{pullup}}{R_{LED}} \text{CTR} \frac{1}{1 + sR_{pullup}\left(C_{opto} \parallel C_2\right)} \tag{7}$$

This statement still holds if you plan to replace the TL431 by a classical op amp, such as the LM358. The circuit is very popular in Constant-Current/Constant-Voltage (CC-CV) configurations for cell phone chargers for instance. In that case, Figure 21 side b, shows that the op amp uses a TL431 as a static voltage reference and biases the LED in a similar way as in Figure 21a. Therefore, the op amp output conveyed to the feedback node V_{FB} also undergoes the transfer function described by (7). What are the preliminary conclusions? The fact that we isolate the fast lane does not shield us from the optocoupler parameters: its CTR still plays a role as its pole does. Therefore, since a pole is unavoidable, we can use it and make it full part of the transfer function we are looking for. If we do not, then the ac transfer function built around the TL431 or an op amp will be affected by this extra pole that we will have to deal with. Our strategy in the following examples is to welcome this pole in the design: welcome home, pole.

Designing a type 2 with the fast lane removed

The type 2 configuration has already been unveiled in Figure 21a. Its design methodology starts with the choice of the Zener diode. What helps to isolate the fast lane is the headroom between the diode breakdown voltage and the rail from which the bias is derived, V_{out}. However, the decoupling can sometimes become an impossible exercise if the output voltage is low. In that case, a circuit as the one described in Ref. [1] can help but it requires an extra winding, sometimes not available. In our example, suppose we regulate a 12-V output. A Zener voltage around 10 V should do the job well, however, in our laboratory, we purposely used a 6.2-V type because of its immediate availability. The 12-V converter we want to stabilize requires a transfer function *G(s)* featuring the following characteristics:

- A 0-dB mid-band gain *G* at 1-kHz crossover frequency
- A zero f_z located at 364 Hz
- A pole f_p placed at 2.75 kHz
- The resistive divider is made of a 38-kΩ resistor for R_1 and a 10-kΩ is connected to ground.

1. We have seen in the previous article that the series resistor R_{LED} was important to make sure the TL431 had enough bias current to operate in good conditions. We can show that the LED resistor cannot exceed a certain value dictated by the following equations:

$$R_{LED,\max} \le \frac{V_z - V_f - V_{TL431,\min}}{V_{dd} - V_{CE,sat} + I_{bias}\text{CTR}_{\min}R_{pullup}} R_{pullup}\text{CTR}_{\min} \tag{8}$$

Where:

V_z, the Zener diode breakdown voltage (6.2 V)
I_{bias}, the TL431 biasing current when the optocoupler LED is paralleled with a resistor (usually 1 kΩ for a 1-mA bias)
$V_{TL431,\min}$, the minimum voltage the TL431 can go down to (2.5 V)
V_f, the optocoupler LED forward drop (≈ 1 V)
$\text{CTR}_{\min}$, the minimum optocoupler current transfer ratio, in our case 30%
$V_{CE,sat}$, the optocoupler saturation voltage (≈ 300 mV at a 1-mA collector current) which imposes the minimum feedback voltage.
V_{dd}, the internal bias of the pull-up resistor, usually 5 V

The numerical result given by (8) is 1.5 kΩ. If we arbitrarily opt for a 50-% margin, the selected value for R_{LED} drops to 750 Ω.

2. To crossover at 1 kHz, the total chain *G(s)* must exhibit a gain of 1 (0 dB) at this frequency. However, *G(s)* is actually made of a compensator $G_1(s)$ whose output crosses the optocoupler chain, also affected by a gain $G_0(s)$. The total gain *G(s)* is therefore the product of both gains $G_1(s)G_0(s)$. Since G_0 is fixed by (6), we can evaluate the value at which the 1-kHz gain must be tailored for G_1 :

$$G_1 = \frac{G}{G_0} = \frac{1}{R_{pullup}} \frac{R_{LED}}{\text{CTR}} = \frac{1}{20k} \frac{750}{0.3} = 0.125 \tag{9}$$

3. The resistor R_2 places the zero, in relationship with C_1. As shown in Ref. [1], this element can be calculated using the following formula:

$$R_2 = \frac{\sqrt{\left(f_z^2 + f_c^2\right)\left(f_p^2 + f_c^2\right)}}{\left(f_z^2 + f_c^2\right)} \frac{G_1 f_c R_1}{f_p} = 4.75\ k\Omega \tag{10}$$

4. From R_2, the zero capacitor C_1 is easily derived:

$$C_1 = \frac{1}{2\pi f_z R_2} = \frac{1}{6.28 \times 364 \times 4.75k} = 92\ nF \tag{11}$$

5. What now is missing is the pole capacitor C_2 which must combine with C_{opto} to form the total value we are actually looking for. This value for C_{tot} is derived from (7):

$$C_{tot} = \frac{1}{2\pi R_{pullup} f_p} = \frac{1}{6.28 \times 20k \times 2.74k} = 2.9\ nF \tag{12}$$

The optocoupler has been characterized and exhibits a pole at 6 kHz. Combined with a 20-kΩ pull-up resistor, it corresponds to a parasitic capacitor C_{opto} of 1.3 nF (use equation (12) where f_p is replaced by the 6-kHz pole). Because C_{opto} and C_2 are in parallel to form C_{tot}, C_2 value is simply:

$$C_2 = C_{tot} - C_{opto} = 2.9n - 1.3n = 1.6\ nF \tag{13}$$

6. Now that all components are calculated, the zener bias resistor R_z must be chosen. The current that crosses it is made of the 1-mA bias current for the TL431, I_{bias}, the LED current I_L necessary to change V_{FB} plus the current biasing the Zener diode, I_z. I_z and I_L are picked by the designer. I_L, however, depends on the CTR of the optocoupler. We can easily show that the maximum LED current obeys the following expression:

$$I_{L,\max} = \frac{V_{dd} - V_{CE,sat}}{R_{pullup} \text{CTR}_{\min}} = \frac{5 - 300m}{20k \times 0.3} = 784\ \mu A \tag{14}$$

To ensure a low dynamic resistance for the 6.2-V Zener diode, the data-sheet of the selected device recommends a 4-mA bias current. Added with the 1-mA current for the TL431, the total current crossing R_z is thus:

$$I_{R_z} = I_{bias} + I_z + I_{L,\max} = 1m + 4m + 784\mu \approx 5.8\ mA \tag{15}$$

The resistor biasing the Zener diode R_z must thus be lower than:

$$R_z < \frac{V_{out} - V_z}{I_{R_z}} < \frac{12 - 6.2}{5.8m} < 1\ k\Omega \tag{16}$$

A 0.1-µF capacitor has been added across the diode to improve the ac rejection of V_{out}.

Testing the ac response

Rather than running a simulation with the above values, we actually built a test fixture to extract the compensator transfer response. We could have done this experiment on a working power supply, but the ambient

noise makes the exercise difficult, especially in low frequency. The main difficulty with a high-gain compensator is to maintain the proper bias point, e.g. a collector voltage around 2.5 V, the middle of its dynamic excursion. Even if you carefully adjust a dc power supply to deliver exactly 12.00 V on the TL431 input and have the optocoupler collector voltage around 2.5 V, there will always be slow temperature drifts and noise that will inexorably push the circuit in its upper or lower stops. Rather than manually tweaking a dc source, why not making the process automatic such as in Figure 22. An op amp, a simple LM358, monitors the collector of the optocoupler and adjusts its output to make it equal to the 2.5-V set point, present on its inverting input. That way, if anything changes, the op amp will automatically tweak the bias point to keep the collector at the right 2.5-V level. A 1000-µF capacitor rolls off the loop gain and ensures the stability of the fixture. A network analyzer monitors V_{out} and V_{FB} to produce the Bode plot we are looking for.

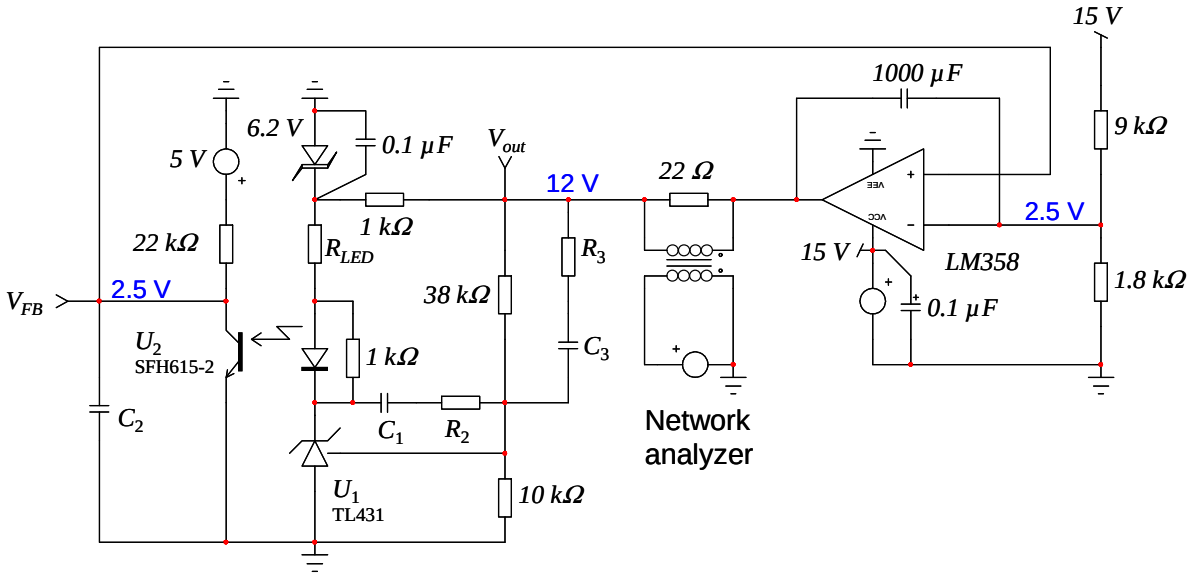

Figure 22: rather than manually fixing the bias point, an op amp does the job automatically by maintaining the right dc voltage on the V_{out} node. R_3 and C_3 are only present for the type 3 study.

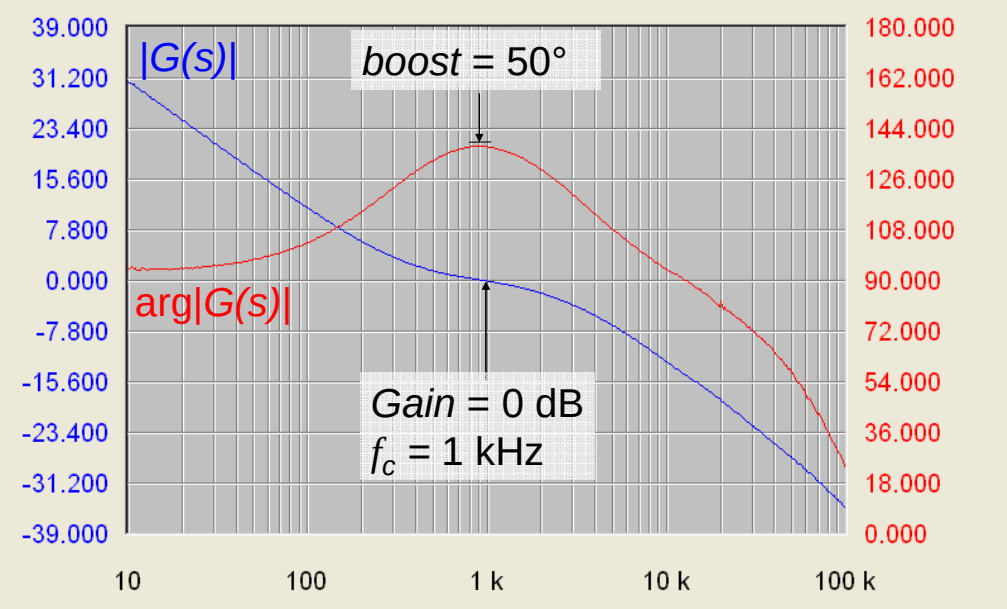

Figure 23: the Bode plot extracted with Figure 22 fixture confirms the type-2 nature of the tested configuration.

As confirmed by Figure 23 plot, we perfectly crossover at 1 kHz with a 0-dB gain. Needless to say that this 0-dB transition would have been impossible to obtain without using the TL431 recommended configuration with the removed fast lane.

Designing a type 3 with the fast lane removed

The type 3 design does not differ that much from that of the type 2. Thanks to the fast lane removal, we just need to add an *RC* network across the upper resistor R_1 and we are all set!

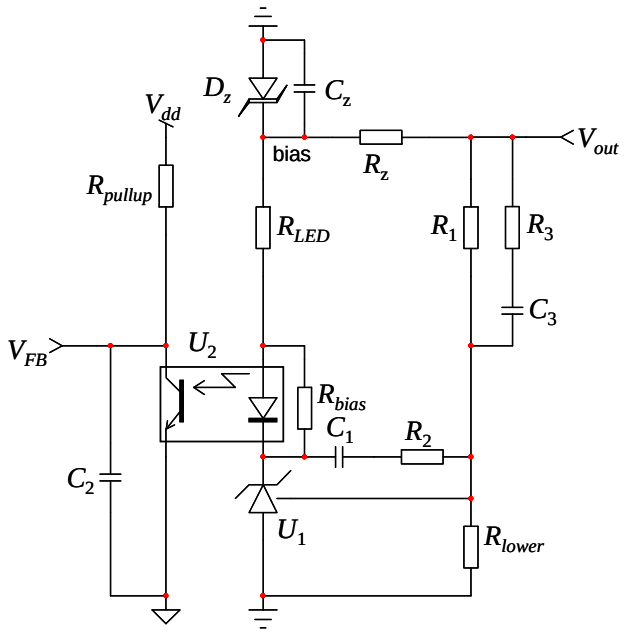

Figure 24: the simple addition of an *RC* network across R_1 turns the compensator in a type 3.

Thanks to the study carried over the type 2, we know that the transfer function of the type 3 is that of the classical op amp configuration multiplied by (7). Therefore, the transfer function of the circuit presented in Figure 24, provided $R_3 << R_1$ obeys the following equation:

$$\frac{V_{FB}(s)}{V_{out}(s)} \approx -\frac{R_{pullup}}{R_{LED}}\text{CTR}\frac{(sR_2C_1+1)(sR_1C_3+1)}{sR_1C_1(1+sR_{pullup}C_2)(sR_3C_3+1)} \tag{17}$$

Once again, let us assume that we need to stabilize a CCM voltage-mode forward converter delivering 12 V. To make it stable, the study of the open-loop Bode plot indicate that the compensator transfer function *G(s)* requires the following parameters combination:

- A 17-dB mid-band gain *G* at 1-kHz crossover frequency
- Two coincident zeros placed at f_z = 200 Hz.
- Two coincident poles placed at f_p = 3 kHz.
- As before, the resistive divider is made of a 38-kΩ resistor for R_1 and a 10-kΩ is connected to ground.
- We assume all the rest of the values (R_{LED}, R_{pullup}, I_{bias} etc.) are similar to that already used in the type 2 example.

Let us follow the steps:

1. The LED series resistor is evaluated using (8) and also leads to a value of 750 Ω.

2. To find the needed mid-band gain pertaining to $G_1(s)$ only, we first evaluate the contribution of the optocoupler chain G_0. For this purpose, we can use (9) again:

$$G_1 = \frac{G}{G_0} = \frac{10^{\frac{17}{20}}}{R_{pullup}}\frac{R_{LED}}{\text{CTR}} = \frac{7.08}{20k}\frac{750}{0.3} = 0.885 \tag{18}$$

3. Resistor R_2 fixes the type 3 mid-band gain. The below formula considers coincident poles and zeros for this case. If there would be a need to split them, the formula turns to a more complex form, as detailed in Ref. [1].

$$R_2 = \frac{f_p^{\,2} + f_c^{\,2}}{f_z^{\,2} + f_c^{\,2}} \frac{G_1 f_c R_3}{f_p} = 8.47\ k\Omega \tag{19}$$

4. Knowing R_2, the series capacitor C_1 can now be evaluated:

$$C_1 = \frac{1}{2\pi f_z R_2} = \frac{1}{6.28 \times 200 \times 8470} = 94\ nF \tag{20}$$

5. The rest of the calculations is straightforward:

$$C_3 = \frac{1}{2\pi f_z R_1} = \frac{1}{6.28 \times 200 \times 38k} = 21\ nF \tag{21}$$

$$R_3 = \frac{1}{2\pi f_p C_3} = \frac{1}{6.28 \times 3k \times 21n} = 2.5\ k\Omega \tag{22}$$

6. The design ends by calculating C_2, which is linked to the pull-up resistor and the optocoupler parasitic contribution:

$$C_2 = \frac{1}{2\pi f_p R_{pullup}} - C_{opto} = 2.6n - 1.3n = 1.3\ nF \tag{23}$$

We are now all set and we can wire these component into the Figure 22 test fixture. The ac sweep results appear in Figure 25 and confirm the validity of our design.

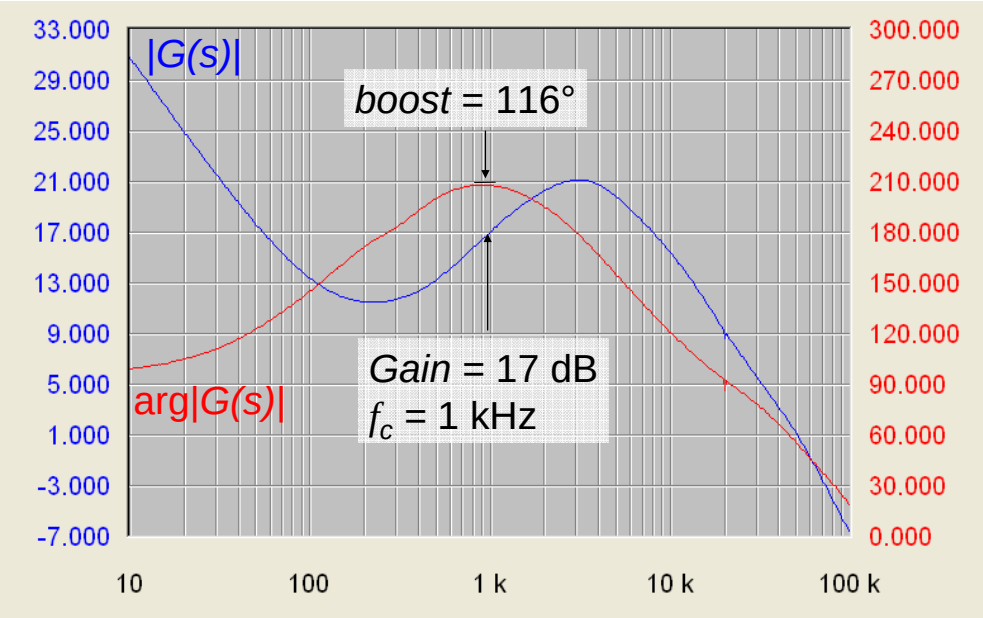

Figure 25: the ac sweep using the test fixture confirms the behavior of a type 3 compensator.

Conclusion

The previous series of articles dedicated to the TL431 have shown the limits brought by the optocoupler configuration and the necessary TL431 bias current. Among the issues, the difficulty to implement a type 3 compensator could be seen as a clear roadblock for the TL431 usage in voltage-mode control applications. Fortunately, this article has shown that a simple zener-based isolation of the fast lane could quickly make the design of TL431-based compensators as easy as their op amp-based counterparts.

References

1. C. Basso, “Switch Mode Power Supplies: SPICE Simulations and Practical Designs”, McGraw-Hill, 2008

The TL431 in Switch-Mode Power Supplies loops: part V

Christophe Basso – ON Semiconductor
14, rue Paul Mesplé – BP53512 - 31035 TOULOUSE Cedex 1 - France

This fifth and last article closes a series of papers dedicated to the TL431 used in loop control applications. Further to the study of the various error amplifier structures built around the device, it is time to show how this knowledge applies to a real case. Several techniques are available to stabilize a converter but among them, we believe the SPICE analysis represents the easiest and quickest path to go. However, in some cases where a simulator is not available, we will show how an automated design tool based on Excel® can efficiently help you to quickly compensate your power supply before actually building the prototype.

Stabilizing a CCM 65-W flyback converter

Popular in the notebook adapters market, the flyback converter operated in current-mode control lends itself very well to low-cost and rugged structures. The typical application of such a converter appears in Figure 26. The controller is a NCP1271 from ON Semiconductor, it operates in fixed-frequency current-mode control and includes a lot of useful features such as a timer-based short-circuit protection, a frequency modulation for an EMI-friendly signature and a skip-cycle function operated in soft mode to meet new standby power requirements at no acoustic noise. Usually, these converters are designed to operate in Continuous Conduction Mode (CCM) at low line to reduce conduction losses but they naturally transition to the Discontinuous Conduction Mode (DCM) of operation at high line. In our example, we will assume that the hardware design is done, implying the selection of the transformer primary inductance L_p, the turns ratio N of the transformer and the rest of the elements: the TL431 is alone, awaiting its compensation elements…

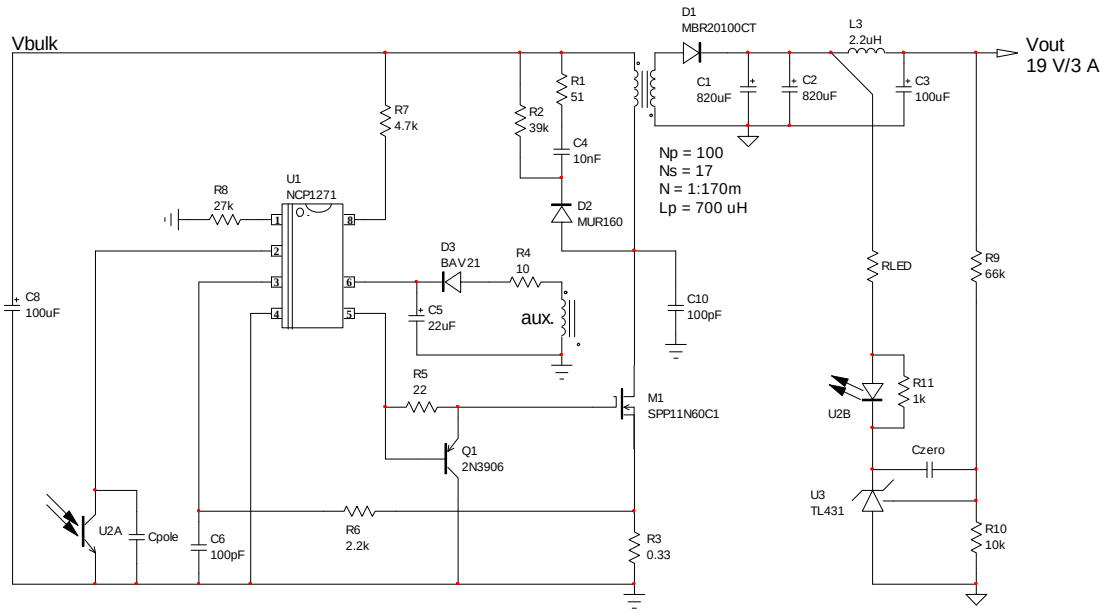

Figure 26: a typical flyback converter using a NCP1271 featuring a frequency-jittered oscillator.

The first thing to do consists in obtaining the control-to-output transfer function of this current-mode flyback converter. This is what is called the open-loop "plant" transfer function. Several options exist to fulfill that goal:

1. Analytically derive the small-signal model of the considered converter and use an automated mathematical tool to extract the magnitude and phase of the power stage response. The equation for the magnitude of a CCM current-mode flyback is rather complicated as indicated by (1). The various poles/zeros appear but also the double sub harmonic poles located at half the switching frequency f_n and affected by a quality coefficient Q_p:

$$\left|H(f)\right| = 20\log_{10}\left[G_0 \frac{\sqrt{1+\left(\frac{f}{f_{z1}}\right)^2}\sqrt{1+\left(\frac{f}{f_{z_2}}\right)^2}\sqrt{1+\left(\frac{f}{f_{z3}}\right)^2}}{\sqrt{1+\left(\frac{f}{f_{p_1}}\right)^2}} \frac{1}{\sqrt{\left(1-\left(\frac{f}{f_n}\right)^2\right)^2+\left(\frac{f}{f_n Q_p}\right)^2}} \right] \quad (1)$$

The phase also needs to be separately computed to make sure a complete Bode plot is generated. The negative sign on the second term of (2) shows that f_{z2} is actually a right half-plane zero (RHPZ):

$$\arg H(f) = \tan^{-1}\left(\frac{f}{f_{z_1}}\right) - \tan^{-1}\left(\frac{f}{f_{z_2}}\right) + \tan^{-1}\left(\frac{f}{f_{z_3}}\right) - \tan^{-1}\left(\frac{f}{f_{p_1}}\right) - \tan^{-1}\left(\frac{f}{f_n Q_p}\frac{1}{1-\left(\frac{f}{f_n}\right)^2}\right) \quad (2)$$

Yes, these formulas imply the separate calculations of all its elements and require great care in computing/plotting the final results. Also, they are only valid for CCM. If your converter transitions to DCM, these expressions need to be updated with new ones, further lengthening the study. If understanding the technique behind the derivation of these results is key for someone who claims to master loop control in switching power supplies, the practical implementation of these formulas is restricted to someone at ease with mathematical analysis.

2. The second option uses a SPICE large or small-signal averaged model. It does not shield you from knowing what hides behind the model, but you no longer need to manipulate tedious equations. A SPICE model first automatically computes the operating point and tells you if the converter operates in CCM or in DCM. It then selects the appropriate equation arrangement and by pressing the start button, you obtain the ac plot in one second.

3. Automated software are another possibility. ON Semiconductor has released an automated spreadsheet that handles all these details for you: populate the component values for L_p, N, input voltage etc., press the update button and you are all set! We will see how it works in few moments...

4. This last option is to build a prototype and try to extract the ac response of the power stage via the use of a network analyzer. This operation is rather easy when you test a power supply whose loop is already stabilized and you want to confirm your calculations by a bench measurement. In case the power supply is not stabilized or barely stable, the task really complicates and risks of fume exist ☺. On the contrary, if you combine options 4 with one of the previous options, you are guaranteed to build a rugged and stable prototype in the smallest amount of time. Yes you can.

Before an average simulation can be performed, a study of the controller internal architecture is necessary. The typical NCP1271 block diagram appears in Figure 27 where the current sense comparator receives the divided feedback information on its inverting input and the current sense signal on its non-inverting input.

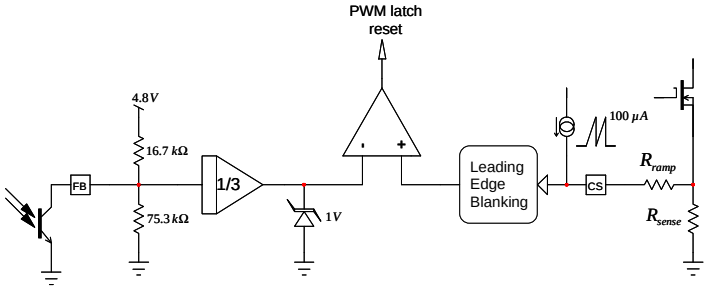

Figure 27: the internal block diagram of the NCP1271 shows that the maximum peak current is precisely clamped to 1 V ± 5%.

The feedback voltage undergoes a divide-by-3 operation to offer a comfortable dynamic range on the optocoupler collector. The primary current read on the CS pin is permanently compared to the feedback signal. It is safely clamped to a precise 1-V level in case of a fault condition: open-loop feedback, short-circuit of the output rails etc. A 180-ns Leading Edge Blanking (LEB) circuit cleanses the current sense signal to remove all spurious oscillations that stray elements or diodes t_{rr} could easily create. In presence of CCM-operated current mode control converters, ramp compensation can be useful to tame the poles located at half the switching frequency. For this purpose, the implementation of such a ramp is simplified owing to a resistor R_{ramp} in series with the current sense pin. This resistor can be tweaked to adjust the level at the desired value. This resistor must be placed very close to the controller and a small 100-pF capacitor from the CS pin to ground will help to further improve the noise immunity of the whole power supply.

A small-signal representation

Now that the internal architecture is understood, let us capture the ac simulation schematic. The power stage together with the TL431-based compensator appear in
Figure 28. For current mode control, a dedicated average model is selected. This subcircuit has been the object of a thorough description in Ref. [1]. It supports the CCM/DCM operating conditions and automatically toggles between them. Thanks to its specific architecture, it operates in dc, transient and ac where sub harmonic oscillations are accurately predicted.

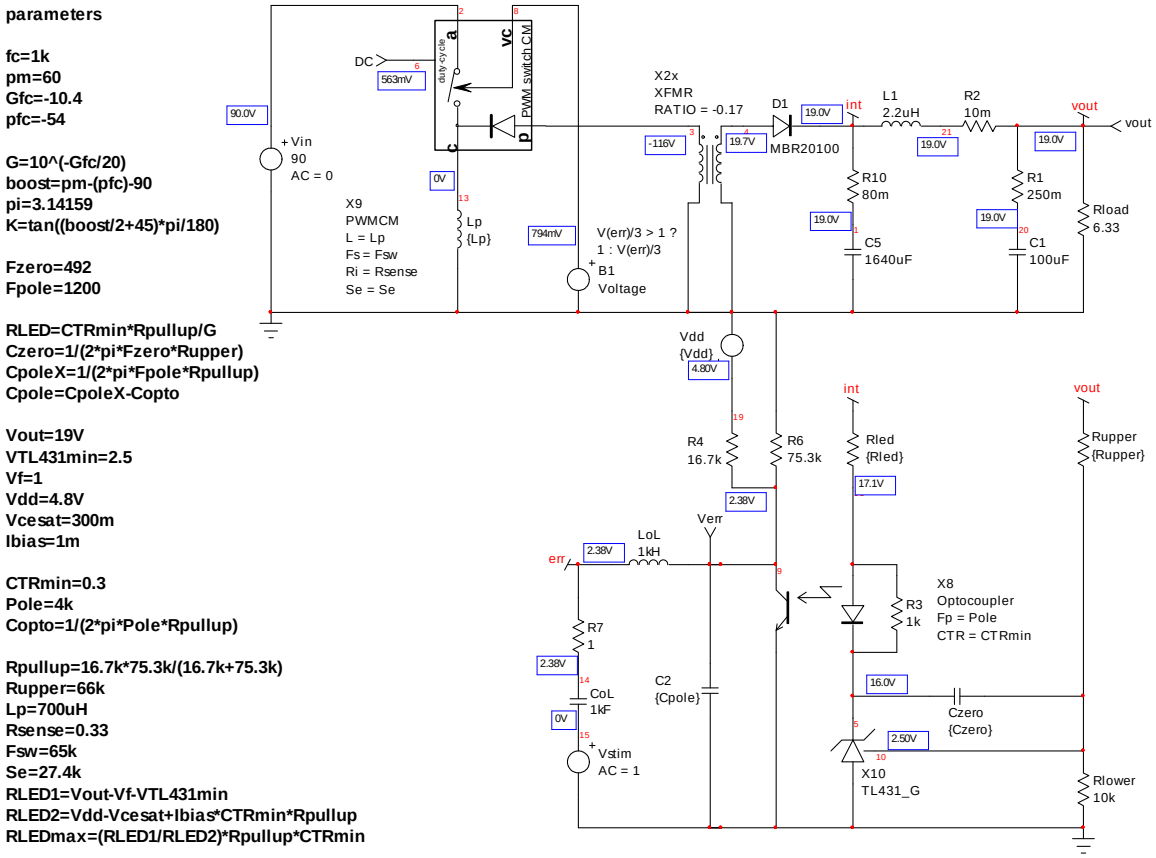

Figure 28: the small-signal representation of our CCM current-mode converter uses an auto-toggling average model.

The divide-by-3 circuitry associated with its 1-V clamp is bundled into an in-line equation which clamps the excursion below 1 V, while dividing the feedback voltage by three. This equation appears in
Figure 28 under the B_1 Analog Behavioral Model (AMB) voltage source in an INTUSOFT's *IsSpice*® syntax. Under Cadence's *PSpice*®, it would be written as follows:

E1 8 0 Value = { IF (V(err/3)>1,1,V(err/3)) }

As shown in **Figure 28**, the dc operating levels are reflected on the schematic. These bias points are calculated by the simulator before any simulation begins. When using average models, check if these bias points correspond to what you expect. In our case, the output voltage is 19 V and the duty-cycle is calculated to 56.2%, this looks correct. The peak current set point is 568 mV over the 0.33-Ω sense resistor which indicates a 1.7-A peak current. Now that our average model gives the correct dc point, we can expect a correct ac response for $H(s)=V_{out}(s)/V_{FB}(s)$ where $V_{FB}(s)$ represents the voltage on the controller feedback pin. The plot appears in Figure 29 and exhibits sub harmonic peaking at half the switching frequency.

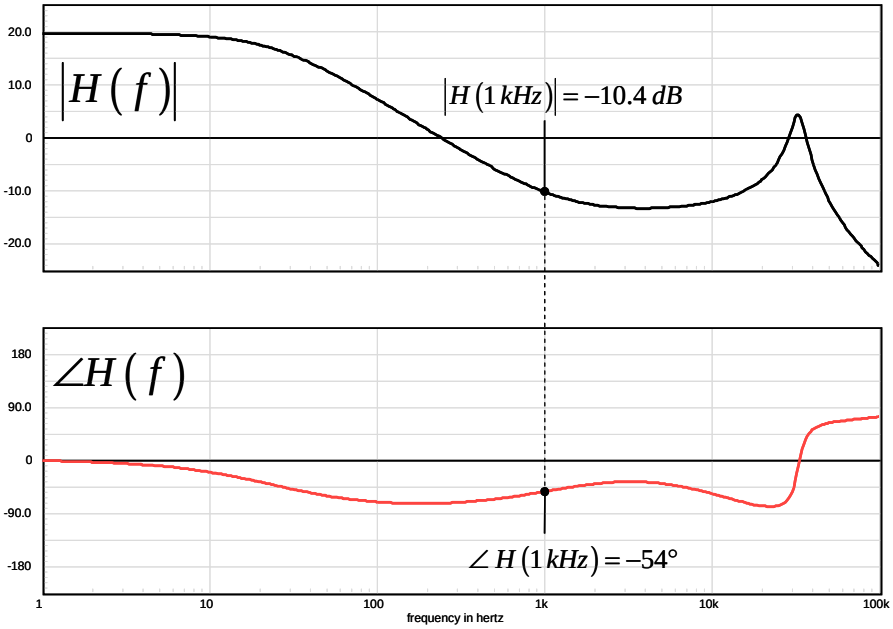

Figure 29: the power stage ac-response shows peaking at half the switching frequency, implying the injection of an external ramp to damp these sub harmonic poles.

This peaking could be quickly damped by injecting ramp compensation. The quickest way is to calculate the primary inductor down slope and inject 50% of it into the model and eventually in the controller. The complete formula is the following, considering the output voltage V_{out}, the primary inductance L_p, the output diode forward drop V_f, the sense resistor R_{sense} and the transformer turns ratio N:

$$S_e = 50\% \left(\frac{V_{out}+V_f}{NL_p} R_{sense} \right) = 0.5 \times \left(\frac{19+0.8}{0.17 \times 700u} \times 0.33 \right) = 27.4\, kV/s \quad (3)$$

Compensating the converter for a 1-kHz bandwidth

Looking at Figure 29, we can see a -10.4-dB attenuation at 1 kHz. Therefore, we must tailor the compensator transfer function *G(s)* to offer +10.4 dB of gain at 1 kHz. Then, some phase boost must be provided to obtain an adequate phase margin once the loop is closed. This phase margin selection depends on numerous criteria among which we have the recovery time and the component dispersions. To make sure our phase margin never goes below the 45-° limit, we can shoot for 60°. To obtain this amount of margin, we need to place poles and zeros such that the compensator *boosts* the phase in the vicinity of the 1-kHz region. How much phase boost shall we provide to reach a phase margin of 60°? Ref. [1] provides a simple formula which cumulates the phase rotations appearing in the compensation loop and calculate the necessary boost to stay away from the limit of -360°:

$$BOOST = \varphi_m - \arg H(f_c) - 90° = 60° + 54 - 90 = 24° \quad (4)$$

In our plant transfer function *H(s)*, we can see the effect of the output capacitor ESR which fights the low frequency pole and improves the phase. To force the gain decrease as we go down the frequency axis, it is customary to place a pole right where the ESR zero occurs:

$$f_{p_1} = \frac{1}{2\pi R_{ESR} C_{out}} = \frac{1}{6.28 \times 80m \times 1.64m} = 1.2\ kHz \tag{5}$$

With a pole located at 1.2 kHz, where do we place the zero to obtain a phase boost of 24°. The closer the pole and zero are, the less phase boost we obtain. Of course, when they coincide, the boost is null and we end up with a pure integrator. An integrator, also called a type 1, is only suitable in cases where no phase boost is required. For instance, if your power stage has a phase rotation below 45° at the crossover frequency, then a type 1 can do the compensation job. In our case, as we need a little bit of phase boost, we need a compensation circuit featuring a pole and zero. It obeys the following transfer function equation:

$$G(s) = \frac{\left(1 + \frac{s}{s_{z_1}}\right)}{\left(1 + \frac{s}{s_{p_1}}\right)} \tag{6}$$

The phase rotation induced by this filter is simply the numerator argument minus the denominator argument:

$$\arg G(f) = \arctan\left(\frac{f}{f_{z1}}\right) - \arctan\left(\frac{f}{f_{p1}}\right) \tag{7}$$

From this equation, we can now solve for the zero position given a 1-kHz crossover, a 1.2-kHz pole position and a wanted phase boost of 24°:

$$f_{z_1} = \frac{f_c}{\tan\left[24° + \tan^{-1}\left(\frac{f_c}{f_{p_1}}\right)\right]} = 492\ Hz \tag{8}$$

Now that we know where to place our pole and zero, let's move to the practical implementation with a TL431 network.

Using the TL431 in a type-2 network

A type 2 compensator appears in Figure 30. The network uses an optocoupler to convey the isolated secondary side information to the primary side controller. This optocoupler needs to be characterized to find where its pole lies. In our case, we have selected a SFH615 which operated at 350-µA collector current (a 4.8-V V_{DD} with an equivalent pull up of $16.7k\Omega \parallel 75.3k\Omega$) shows an equivalent pole around 4 kHz. It equivalent emitter-collector capacitor is therefore:

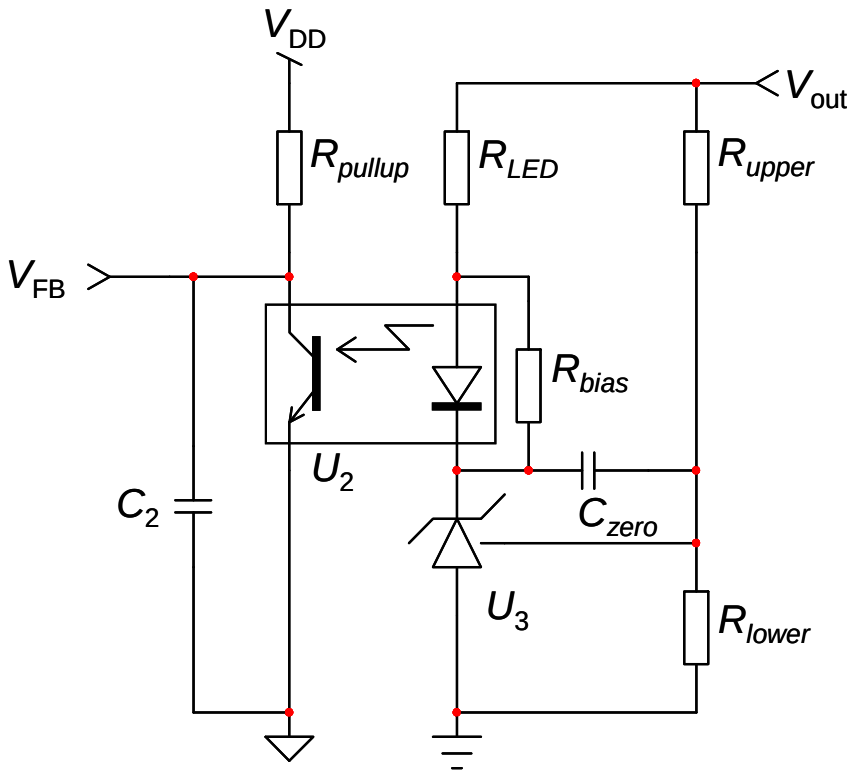

Figure 30: a type 2 compensator with a TL431 combines an origin pole, a zero and a high frequency pole.

$$C_{opto} = \frac{1}{2\pi \times 4k \times 16.7k \,||\, 75.3k} = 2.9\ nF \tag{9}$$

We must place a zero at 492 Hz and a pole at 1.2 kHz. The equations ruling the zero and the pole definitions appear below. They involve the upper resistor bringing V_{out} to the TL431, R_{upper}, as well as the equivalent pull up resistor R_{pullup}:

$$C_{zero} = \frac{1}{2\pi R_{upper} f_{z_1}} = \frac{1}{6.28 \times 66k \times 492} \approx 4.9\ nF \tag{10}$$

$$C_{pole} = \frac{1}{2\pi f_{p_1} R_{pullup}} = \frac{1}{6.28 \times 1.2k \times 13.6k} \approx 9.7\ nF \tag{11}$$

However, C_{pole} is made of C_2 combined with C_{opto}. As C_{opto} is 2.9 nF, C_2 is simply:

$$C_2 = C_{pole} - C_{opto} = 9.7n - 2.9n = 6.8\ nF \tag{12}$$

Finally, the LED series resistor characterizes the mid-band gain necessary to cross over at the selected 1-kHz frequency. In a TL431 arranged in type 2, the mid-band gain is defined by:

$$R_{LED} = \frac{R_{pullup}\text{CTR}}{G_0} = \frac{13.7k \times 0.3}{10^{\frac{10.4}{20}}} = 1.24\ k\Omega \tag{13}$$

The extra resistor, R_{bias}, ensures the circulation of a certain amount of current in the TL431. Adopting a value of 1 kΩ makes the adjustable reference operate as per the data-sheet recommendations which state a 1-mA minimum bias current. Given this extra bias on the LED resistor, we have to make sure that (22) gives us a result compatible with the minimum bias voltage conditions of the TL431 ($V_{TL431,min}$ >> 2.5 V). It can be shown that the LED resistor must stay below a certain value to satisfy this requirement:

$$R_{LED,\max} \le \frac{V_{out} - V_f - V_{TL431,\min}}{V_{dd} - V_{CE,sat} + I_{bias}\mathrm{CTR}_{\min} R_{pullup}} R_{pullup}\mathrm{CTR}_{\min}$$
$$R_{LED,\max} \le \frac{19 - 1 - 2.5}{4.8 - 0.3 + 1m \times 0.3 \times 13.6k} \times 0.3 \times 13.6k \le 7.4\ k\Omega \quad (14)$$

In our case, we have enough margin to ensure sufficient voltage across the TL431 in all operating conditions. The situation really worsens in low output voltage cases: you are almost forced to adopt a type 1 configuration where the LED resistor is calculated solely on bias considerations.

As you can see in the left side of **Figure 28**, we have automated all these calculations thanks to the macro possibilities of INTUSOFT's *SpiceNet*®. This feature also exists in Cadence's *OrCAD*® and helps to quickly experiment various pole/zero combinations. Once the loop has been compensated, we can check the final transfer function at low and high line to make sure our phase margin still exists. This is what Figure 31 confirms.

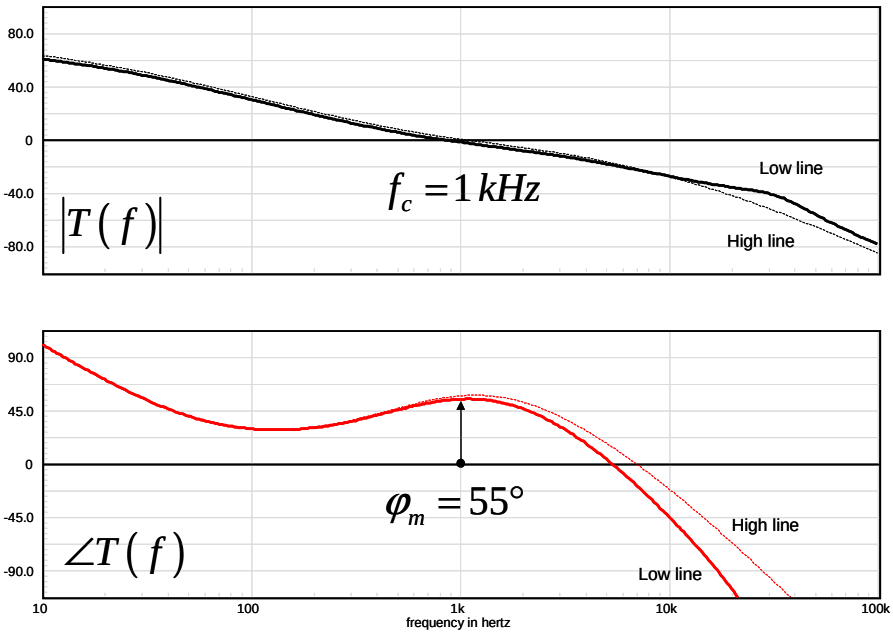

Figure 31: once compensated, the converter exhibits a 1-kHz crossover frequency together with a comfortable phase margin.

An new automated tool

As you read in the previous lines, compensating our flyback converter requires a minimum knowledge of control loop theory. Of course, you could also go to the laboratory and try to play with the resistors and capacitors values until the step response looks good. Well, it reminds me some of the visits I made at customers sites where I saw this kind of approach. Despite the warnings I expressed, the boards went to production. As expected, a few months later, the production line went down, facing un-expected instabilities at final test! If you do not have the time to derive the equations, why not looking for an automated tool that does all the math for you? This is exactly what we thought when we developed this Excel®-based spreadsheet featuring several separated tabs, starting from the component values up to the final bill of material. Just enter the component values for the converter section and press ok. You should see the power stage response as illustrated in Figure 32 (right side), confirming the peaking and the CCM operation. The duty-cycle is 55% and the gain flattens to 19.6 dB at dc, what we also did see in Figure 29.

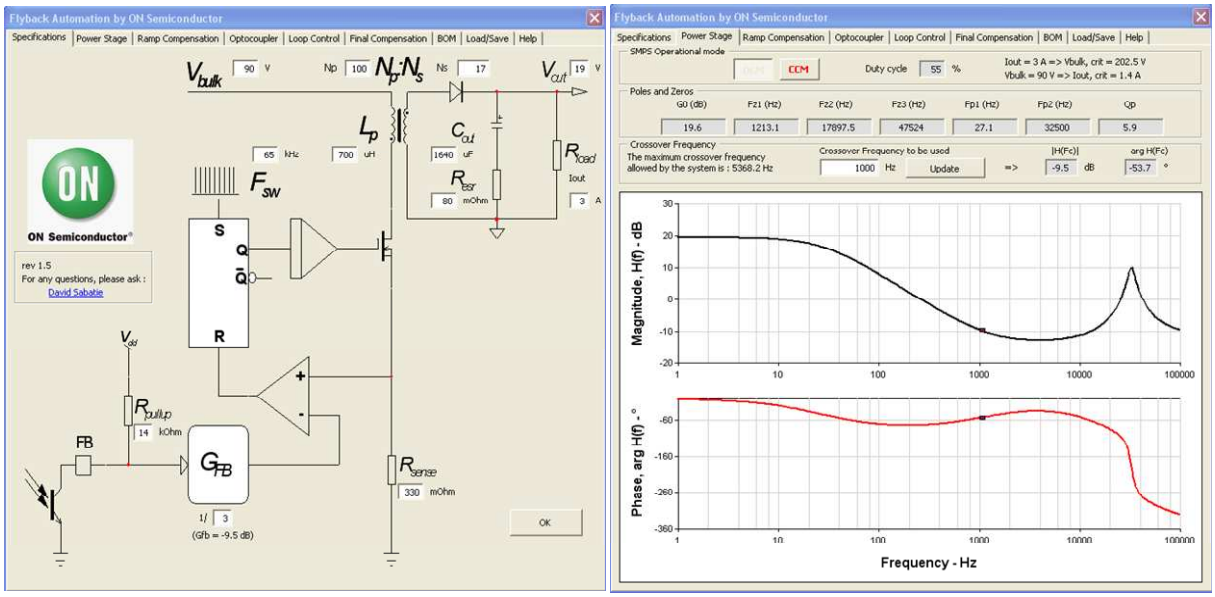

Figure 32: the left-side opening screen invites you to fill up the component values you have calculated. Once you press ok, the power stage tab appears and unveils the power stage ac response (right).

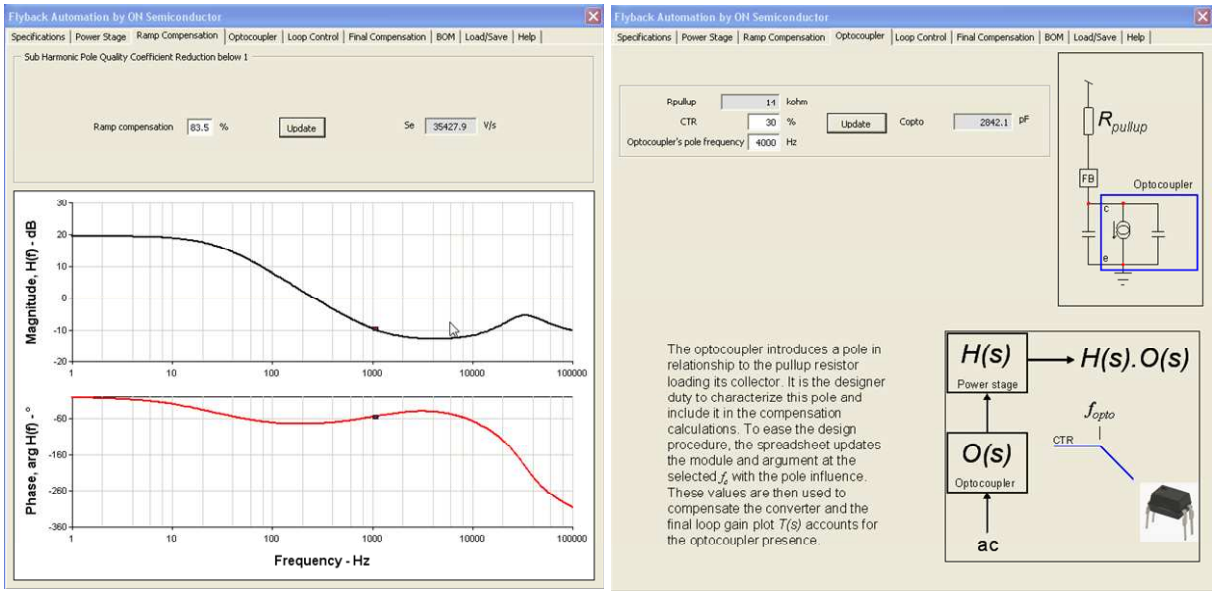

Figure 33: the next step is to evaluate the necessary amount of ramp compensation and its effect on the power stage response. Then the optocoupler tab shows up and lets you enter the measured pole.

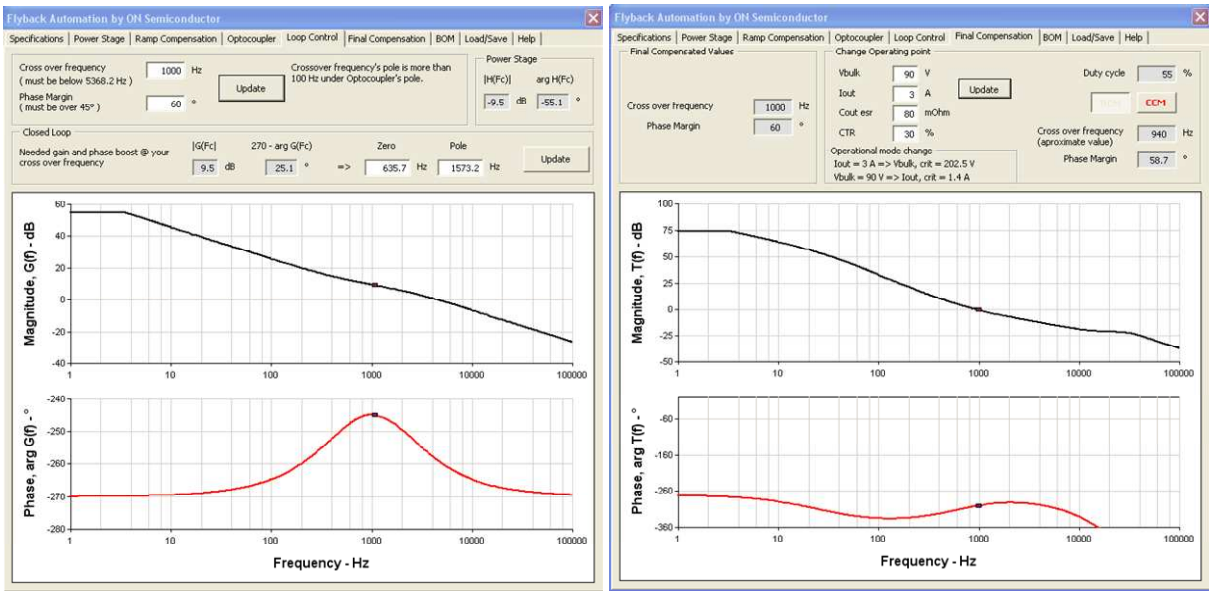

Figure 34: the proposed compensator for a 60-° phase margin on the left, shows a boost of 25°, very close to what we calculated. Once compensated, the resulting phase margin corresponds to our wishes (right).

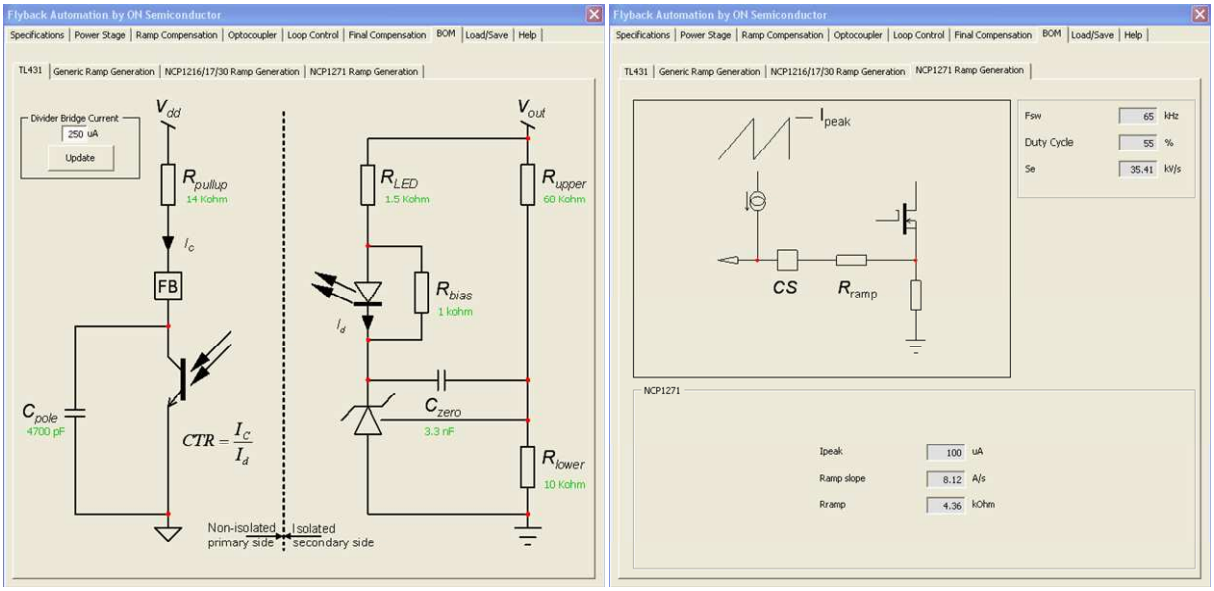

Figure 35: the software eventually shows you the TL431 configuration with its associated component (left). It also teaches you how to implement ramp compensation either generically or by using the internal NCP1271 circuitry (right).

The software then damps the sub harmonic poles by selecting the right amount of compensation ramp (Figure 33). The method employed here differs from that used in (3). The spreadsheet calculates the equivalent quality coefficient Q_p and checks how much ramp compensation is necessary to reduce it below 1. In theory, it reduces the risk of over compensation given by (3) in which is considered a duty-cycle excursion up to 100%. Then, the user is required to enter the optocoupler characteristics consisting of a Current Transfer Ratio (CTR) and a pole whose position depends on the pull-up or pull-down resistor. In the given example, the CTR is 30% whereas the pole was found to be at 4 kHz. A tutorial available with the software details how to characterize the optocoupler and it's role must be well understood when designing the power supply.

As Figure 34 depicts, the type 2 compensator offers the needed 25-° boost by placing a zero at 635 Hz and a pole at 1.5 kHz (left). The software implements the *k* factor technique which consists in placing the crossover frequency in the geometric means of the selected pole and zero. Finally, as confirmed by Figure 34 right side, the loop gain exhibits a crossover point close to 1 kHz with an adequate phase margin. A button on the upper right corner lets you change the operating points, in particular the input voltage and the output current.

When the update button is pressed, the software recomputes the power stage characteristics, keeping the compensator parameters constant. It then displays the loop gain, accounting for the changes you asked. You can then quickly check if the power supply remains stable when it transitions from CCM to DCM for example. Output capacitor Equivalent Series Resistor (ESR) and optocoupler CTR are among the parameters that can also be swept.

At the end, Figure 35 offers a view of the TL431 and all its calculated values. The right panel indicates ways to practically implement ramp compensation. As a NCP1271 was selected, the insertion of a simple resistor from the sense element to the current-sense pin does the job instantaneously. As previously underlined, it is best to team up this resistor with a 100-pF capacitor to ground for an improved noise immunity at the current sense pin. Both components will be located close to the controller pins.

We have carried several experiments to check the validity of the compensation strategy adopted in the spreadsheet. Experience shows that the final results collected on the bench with a network analyzer are very close to the final goal. Most of the discrepancies come from the capacitors ESR or the optocoupler characteristics. Pay good attention to those before running the software and loop control will no longer be a headache for you! The spreadsheet can be downloaded following Ref. [2] link.

Conclusion

This article closes our series on the TL431 and its usage in the loop compensation of switching power supplies. This guided tour showed the need to understand the parameters involved in the design of a proper compensator based on this popular shunt regulator. If design software or simulation tools can quickly suggest a working circuit, it is your interest to understand the analytical steps behind compensator calculations. This way, not only you can challenge the delivered results and detect a flaw in your approach, but you can also improve the final result by giving the emphasis on a given parameter whose importance is high to your designer eyes. This is the recipe to success!

References

4. C. Basso, “Switch Mode Power Supplies: SPICE Simulations and Practical Designs”, McGraw-Hill, 2008
5. http://www.onsemi.com/pub/Collateral/FLYBACK%20AUTO.ZIP